A Fully Integrated Single-BJT-Based Temperature-to-Digital Converter Achieving ±0.23 °C (3σ) Over 2.0–5.5 V for Duty-Cycled Operation

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***Abstract*—This article presents a fully integrated temperature-to-digital converter (TDC) fabricated in a 0.18 μm CMOS process, employing a single bipolar junction transistor (BJT). The proposed front-end sequentially biases a single BJT at two current levels to generate a ΔV_{BE}, thereby eliminating the need for matched BJT pairs and improving reproducibility with a one-point calibration. All critical analog and digital blocks—including the sensing front-end, an incremental delta-sigma analog-to-digital converter, power management units (PMUs), clock generators, e-fuse memory, digital processing logic, and an I^2C interface—are fully integrated on-chip to enable compact and standalone operation. After one-point calibration at 30 °C, the TDC achieves an inaccuracy of ±0.23 °C (3σ) over a −40 °C to 125 °C temperature range. At a conversion time of 7.68 ms, it achieves a 6.71 mK rms resolution, corresponding to a system-level resolution figure of merit (FoM) of 75.3 pJ · K^2. For the sensing core, the resolution FoM is 11.8 pJ · K^2. A co-integrated dual-BJT TDC exhibits an inaccuracy of ±0.37 °C (3σ), validating the effectiveness of the single-BJT approach for comparison. The TDC operates from a 2.0 to 5.5 V supply with low supply sensitivity of 2.54 m°C/V and supports a low standby current of 420 nA at 2.0 V, enabling compact size, high accuracy, and energy efficiency for duty-cycled applications.**

***Index Terms*—Delta-sigma ADC, duty-cycled applications, fully integrated sensor, low-power, mismatch mitigation, single-bipolar junction transistor (BJT)-based architecture, standby state, temperature-to-digital converter (TDC), wide supply voltage.**

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I. Introduction

ACCURATE temperature sensing is critical in IoT devices, wearable sensors, and thermal management of advanced SoCs [1]. With the growth of IoT and wearable applications, there is substantial demand for temperature-to-digital converters (TDCs) that are both highly accurate and energy-efficient [2], [3]. Among various on-chip temperature sensing approaches, including those based on bipolar junction transistors (BJTs), metal-oxide-semiconductor (MOS) transistors, and resistors, BJT-based sensors are widely adopted due to their high linearity, long-term stability, and compatibility with standard CMOS processes, enabling accurate and reproducible measurement often with only one-point calibration [4], [5], [6], [7]. In contrast, MOS-based sensors, which exploit the temperature dependence of gate-to-source voltage in subthreshold operation, typically offer lower power consumption and smaller area but suffer from higher inaccuracy and require multiple trimming points to achieve comparable performance [8]. Resistor-based sensors leverage the thermal coefficients of integrated resistors to enable energy-efficient designs, but they are sensitive to process variations and often require extensive calibration [9]. This work focuses on a BJT-based approach to balance accuracy, calibration simplicity, and integration.

Conventional BJT-based TDCs typically employ two matched BJTs to generate a proportional-to-absolute-temperature (PTAT) ΔV_{BE} [10], [11], [12]. One of the most common readout architectures is the indirect delta-sigma ($\Delta\Sigma$) approach, in which V_{BE} and ΔV_{BE} are combined in the analog domain to generate a temperature-dependent [10], [13]. More recently, digital-assisted readout schemes have emerged that directly digitize $V_{BE}/\Delta V_{BE}$ or $k \cdot \Delta V_{BE}/V_{BE}$ and then compute temperature in the digital domain, reducing analog complexity and improving scalability [14], [15]. Furthermore, these schemes use single-point calibration to digitally correct for both the spread and nonlinearity of V_{BE}, thereby avoiding the complexity and potential nonidealities of analog trimming circuits. However, ΔV_{BE} errors arising from mismatches in the sensing elements persist, as such mismatches are not fully compensated by a single-point calibration and thus fundamentally limit the achievable accuracy.

To mitigate inaccuracies arising from a mismatch between sensing elements, techniques such as dynamic element matching (DEM) or swapping are often employed. These methods average out mismatch errors over time but do not eliminate them. A more fundamental approach is to eliminate the source of the mismatch using a single sensing element. For example, in MOS-based sensors, mismatch can be avoided by utilizing a single MOS transistor as the sensing element, as discussed in [16].

This work presents a single-BJT-based architecture that generates a ΔV_{BE} by sequentially biasing one PNP BJT at two current levels. This technique eliminates errors from device pairs, enabling high accuracy over a wide temperature and supply range with only a single-point calibration. Furthermore, the design enhances precision and saves area by directly coupling the front-end to the incremental $\Delta\Sigma$ ADC, which removes intermediate interface circuits and their potential error sources. For a compact, standalone solution tailored to intermittently operated systems, the TDC is fully integrated, incorporating all critical blocks on a single chip: the sensing front-end, an incremental $\Delta\Sigma$ ADC, on-chip power management units (PMUs), oscillators, e-fuse memory, digital processing, and an I^2C interface. This high level of integration enables robust operation over a wide 2.0–5.5 V supply and a low-power standby state for energy-efficient, duty-cycled conversions.

This article makes the following contributions.

1) A single-BJT sequential-bias architecture that removes inherent mismatch while supporting straightforward one-point calibration.
2) A fully integrated implementation that includes all analog/digital blocks and on-chip PMUs for supply-invariant operation across 2.0–5.5 V.
3) System-level techniques—DEM, chopping, correlated double sampling (CDS), and a dual-mode low-dropout (LDO) regulator—that together enable 2.54 m°C/V supply sensitivity and a 420 nA standby state at 2.0 V.
4) Measured performance of ±0.23 °C (3σ) inaccuracy from −40 °C to 125 °C after single-point calibration and 6.71 mK rms resolution at a conversion time of 7.68 ms; a co-integrated dual-BJT configuration shows ±0.37 °C (3σ).

The remainder of this article is organized as follows. Section II reviews conventional BJT-based TDC architectures and their calibration and mismatch issues. Section III describes the proposed single-BJT sensing approach and integrated power management. Section IV details the circuit implementation and precision enhancement techniques. Section V presents measurement results, and Section VI concludes this article.

II. Background

A. TDC Readout Topologies

Fig. 1 shows a conventional BJT-sensor front-end in which two BJTs, Q_1 and Q_2, are biased at different current densities to generate V_{BE1} and V_{BE2}

$$V_{\mathrm{BE1}} = \frac{kT}{q} \cdot \ln\left(\frac{I_{BIAS}}{I_{\mathrm{S}}}\right),\ V_{\mathrm{BE2}} = \frac{kT}{q} \cdot \ln\left(\frac{N \cdot I_{BIAS}}{I_{\mathrm{S}}}\right) \quad (1)$$

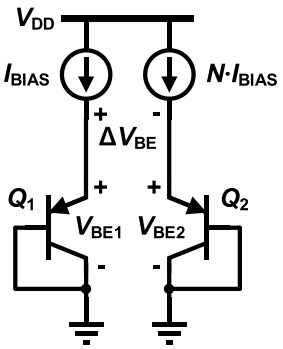


Fig. 1. Conventional BJT-based TDC front-end structure generating the V_{BE} and the ΔV_{BE}.

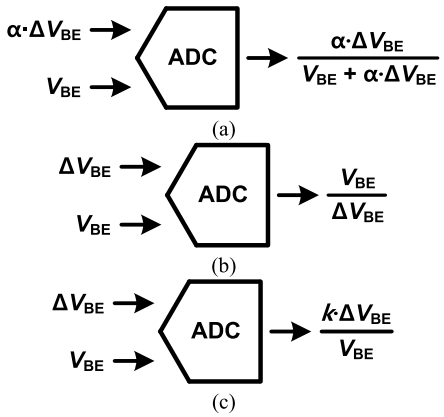


Fig. 2. TDC readout topologies. (a) Classical indirect readout topology. (b) Digitally assisted topology with the ratio $X = V_{\mathrm{BE}}/\Delta V_{\mathrm{BE}}$. (c) Digitally assisted topology with the ratio $Y = k \cdot (\Delta V_{\mathrm{BE}}/V_{\mathrm{BE}})$.

so that their difference is a PTAT quantity

$$\Delta V_{\mathrm{BE}} = \frac{kT}{q} \cdot \ln(N). \quad (2)$$

After V_{BE} and ΔV_{BE} are generated in the front-end, they are digitized and processed to yield a temperature estimate. Depending on how these quantities are combined and digitized, readout topologies can be grouped into three categories as illustrated in Fig. 2.

Fig. 2(a) shows the classical indirect readout topology, where the analog front-end directly generates an analog ratio defined as $\alpha \cdot \Delta V_{\mathrm{BE}}/(V_{\mathrm{BE}} + \alpha \cdot \Delta V_{\mathrm{BE}})$, which is then digitized by an ADC [10], [17]. This approach inherently yields a digital output linearly proportional to temperature, thereby minimizing the complexity of digital postprocessing. Additionally, by designing the reference voltage to exhibit a slight PTAT characteristic, overall TDC inaccuracy can be effectively reduced. However, realizing this functionality entirely in the analog domain is often inefficient, as it entails a large silicon area overhead and is susceptible to gain errors, offset variations, and PVT fluctuations.

Fig. 2(b) illustrates a readout topology in which the analog ratio $X = V_{\mathrm{BE}}/\Delta V_{\mathrm{BE}}$ is directly digitized by an ADC, typically implemented as a zoom ADC [15], [19]. This digitized ratio X is subsequently processed digitally to yield a linear

temperature-dependent digital value (μ)

$$\mu = \frac{\alpha}{\alpha + X}. \tag{3}$$

This digitally assisted approach simplifies analog front-end design by digitally trimming the coefficient α. However, this approach requires a large number of capacitive elements in the ADC's capacitor digital-to-analog converter (CDAC), increasing silicon area and susceptibility to capacitor mismatch. Moreover, the inherently limited ADC input signal range relative to the reference voltage renders this architecture less suitable for applications involving multisensor integration [20].

Alternatively, Fig. 2(c) illustrates a readout topology in which the ADC digitizes an amplified inverse ratio defined as $Y = k\cdot(\Delta V_{\mathrm{BE}}/V_{\mathrm{BE}})$ [14], [20]. Since ΔV_{BE} is smaller than V_{BE}, a gain factor k (typically between 4 and 8) is introduced in the analog domain to amplify the small ΔV_{BE} signal, thereby efficiently utilizing the ADC input dynamic range. The digitized ratio Y is subsequently converted into μ

$$\mu = \frac{\alpha \cdot Y}{\alpha \cdot Y + k}. \tag{4}$$

This configuration inherently ensures that the ADC reference remains larger than the sensing input, simplifying integration with standard switched-capacitor ΔΣ modulators and making it well-suited for applications involving multisensor integration. It also reduces the number of capacitors required, saving silicon area and mitigating mismatch issues. Moreover, digital trimming is straightforwardly supported without added analog complexity.

B. V_{BE} Spread Correction

Compared to ΔV_{BE}, which is PTAT and relatively insensitive to global process variations, the V_{BE} exhibits CTAT characteristics and is significantly more sensitive to process variations [10]. This sensitivity mainly arises from variations in the I_{BIAS} and the I_{S}. If uncorrected, these variations result in significant device-to-device temperature offsets. Including these process-induced spreads, the base–emitter voltage can be expressed as follows:

$$\begin{aligned} V_{BE} &= \frac{kT}{q}\cdot \ln\left(\frac{I_{BIAS}\cdot\left(1+\delta_{I_{BIAS}}\right)}{I_S\cdot\left(1+\delta_{I_S}\right)}\right) \\ &= \frac{kT}{q}\cdot \ln\left(\frac{I_{BIAS}}{I_S}\right) + \frac{kT}{q}\cdot \ln\left(\frac{1+\delta_{I_{BIAS}}}{1+\delta_{I_S}}\right) \end{aligned} \tag{5}$$

where δ_{IBIAS} and δ_{IS} represent the relative errors in the I_{BIAS} and the I_{S}, respectively.

As (5) indicates, the process-dependent spread in V_{BE} can be mitigated by compensating the PTAT component embedded in V_{BE} [18]. Depending on the readout topology, this compensation procedure can be realized in the analog front-end or digital back-end, as detailed in Section II-C.

C. Calibration Method

In classical indirect readout topologies such as Fig. 2(a), trimming the V_{BE} for PTAT correction typically involves applying a programmable PTAT voltage in the analog front-end [10], [21]. This is commonly realized by programming the transistor's bias current with a ΔΣ current digital-to-analog converter (DAC) [10].

Alternatively, in the digitally assisted inverse-ratio readout approach depicted in Fig. 2(c), PTAT correction can be performed without additional analog trimming hardware [14]. In this topology, the amplified inverse ratio $Y = k\cdot(\Delta V_{\mathrm{BE}}/V_{\mathrm{BE}})$ is digitized, and by defining $Z = 1/Y$, the temperature-dependent code μ can be described as follows:

$$\mu = \frac{(\alpha/k)}{(\alpha/k) + Z}. \tag{6}$$

Adding a digital offset ΔZ to Z yields the trimmed output given by

$$\begin{aligned} \mu &= \frac{(\alpha/k)}{(\alpha/k) + (Z + \Delta Z)} \\ &= \frac{(\alpha/k)\cdot \Delta V_{BE}}{(\alpha/k)\cdot \Delta V_{BE} + V_{BE} + \Delta Z\cdot \Delta V_{BE}}. \end{aligned} \tag{7}$$

As shown in (7), PTAT correction can be performed digitally through a straightforward arithmetic operation involving the product term $\Delta Z\cdot\Delta V_{\mathrm{BE}}$, eliminating the need for extra analog complexity.

D. BJT Mismatch

While the spread in V_{BE} can be corrected by one-point calibration, the variation in ΔV_{BE} due to device mismatch is not fully compensated by single-point calibration and thus directly impacts TDC inaccuracy. In conventional BJT-based TDCs, the signal is derived from two closely placed and nominally identical BJTs. In such configurations, global process variations are largely canceled, and the dominant source of ΔV_{BE} error arises from local mismatch between the two devices.

To analyze the impact of local BJT mismatch, this work considers the variation in saturation current I_{S} as a key factor. The resulting ΔV_{BE} incorporating this mismatch can be expressed as follows:

$$\Delta V_{\mathrm{BE}} + \varepsilon_{BJT} = \frac{kT}{q}\cdot \ln\left(N\cdot\left(1+\varepsilon_{I_S}\right)\right) \tag{8}$$

where $\varepsilon_{\mathrm{IS}}$ denotes the relative mismatch in I_{S} between the two BJTs, and $\varepsilon_{\mathrm{BJT}}$ is the resulting voltage error, given by

$$\varepsilon_{BJT} = \frac{kT}{q}\cdot \ln\left(1+\varepsilon_{I_S}\right). \tag{9}$$

After applying the single-point calibration described in (7), the output μ becomes

$$\mu = \frac{(\alpha/k)\cdot(\Delta V_{BE} + \varepsilon_{BJT})}{(\alpha/k)\cdot(\Delta V_{BE} + \varepsilon_{BJT}) + V_{BE} + \Delta Z\cdot\Delta V_{BE}}. \tag{10}$$

As shown in (10), the digital offset ΔZ effectively corrects for the V_{BE} spread in the denominator; however, the mismatch error term $\varepsilon_{\mathrm{BJT}}$ in the numerator remains uncompensated and thus directly impacts the TDC's inaccuracy.

In the employed process, $\varepsilon_{\mathrm{IS}}$ is approximately 0.088% (1σ). Assuming an uncorrelated mismatch with the temperature sensitivity of ΔV_{BE} shown in Fig. 3, the resulting mismatch between two BJTs leads to a ΔV_{BE} error of approximately

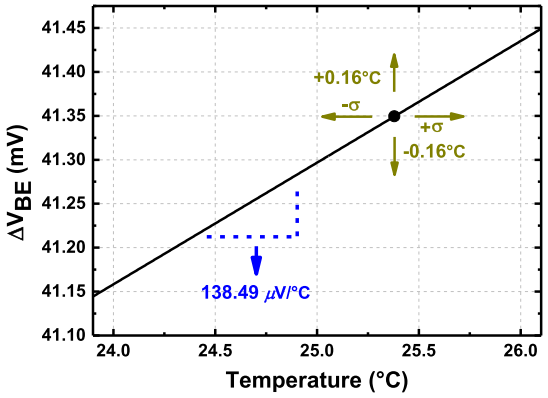


Fig. 3. Simulated temperature sensitivity of ΔV_{BE}, highlighting the impact of BJT mismatch on temperature error.

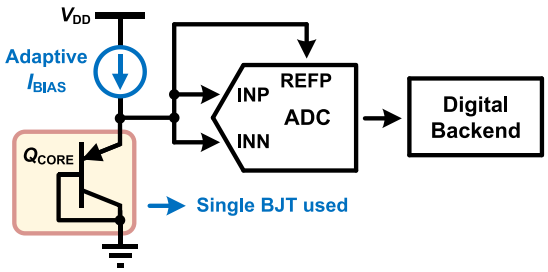


Fig. 4. Simplified block diagram of the proposed single-BJT-based TDC architecture.

0.16 °C (1σ) when $N = 5$. Although the impact of mismatch can be substantially reduced through the use of dummy structures and careful layout techniques, a residual mismatch component that is not fully addressed by a single-point calibration remains, posing a nonnegligible limitation on the achievable TDC accuracy.

III. Proposed Architecture and Operation of TDC

A. Single-BJT-Based Architecture

Fig. 4 shows the simplified block diagram of the proposed single-BJT-based architecture. Unlike conventional TDC architectures that utilize two matched BJTs to generate a PTAT ΔV_{BE}, the proposed approach employs a single BJT. By sequentially biasing the BJT at two current densities, I_S is canceled out, and mismatch-related inaccuracies inherent in transistor pairs are effectively eliminated, enhancing temperature measurement accuracy without requiring additional complex trimming procedures.

The operating principle of the proposed single-BJT-based front-end is illustrated in Fig. 5. Fig. 5(a) depicts the timing diagram of the bias currents applied to the single-BJT. At instant A, the single BJT is biased with the current I_{BIAS}, while at B and C, the bias current is increased to $N \cdot I_{BIAS}$. Each biasing condition yields a different V_{BE} value. As detailed in Fig. 5(b), the voltages sampled at A, B, and C are sequentially applied to the ADC's negative input (INN), positive input (INP), and positive reference input (REFP), respectively. The ADC digitizes these voltages to produce a digital representation proportional to the ratio $k \cdot \Delta V_{BE}/V_{BE}$.

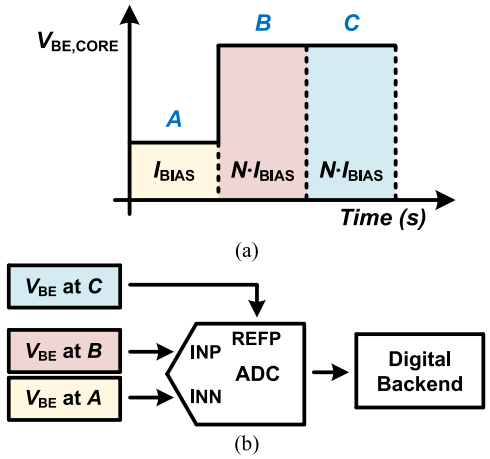


Fig. 5. Operating principle of the proposed single-BJT front-end. (a) Timing diagram of how the bias current is applied to the single BJT. (b) Sampling scheme for ADC input voltages.

In particular, the C-phase (high-current $N \cdot I_{BIAS}$) sample is used as REFP, ensuring the ADC reference remains larger than the sensed input. Since temperature signals inherently exhibit very low-frequency (near-DC) behavior, A, B, and C can be regarded as taken at the same temperature provided the sampling frequency is sufficiently high.

By generating ΔV_{BE} through sequentially biasing the Q_{CORE} at two distinct current levels, the mismatch effects between separate BJTs are inherently canceled. Specifically, this single-BJT approach ensures that ε_{IS} in (8) is effectively zero. As defined by (9), this nullifies the resulting mismatch voltage error ε_{BJT}. As a result, variations stemming from interdevice mismatch, which typically impose accuracy limitations in conventional dual-BJT configurations, are effectively eliminated. This intrinsic cancellation enhances measurement accuracy and ensures improved consistency and reproducibility across multiple fabricated devices.

B. Power Management

For applications that demand energy-efficient duty-cycled operation, compact implementations, and robust operation across varying supply voltages, fully integrated solutions are crucial. By combining the sensing front-end, ADC, PMUs, oscillators, nonvolatile memory, digital processing logic, and digital interfaces on chip, this work achieves high-energy efficiency, reliable performance despite supply fluctuations, and reduced reliance on external circuit components.

Fig. 6 shows the overall architecture of the proposed TDC, organized by power domains. The core blocks are implemented using 1.8 V thin-oxide devices, while the PMU utilizes 5.0 V thick-oxide devices. An on-chip LDO supports a wide 2.0–5.5 V input range, ensuring internal-supply stability by suppressing supply noise. The PMU, implemented with 5.0 V thick-oxide devices, requires a minimum input voltage of 2.0 V for stable operation of its internal circuitry. This minimum supply condition provides a 200 mV dropout to ensure the LDO reliably generates the 1.8 V core voltage. Two

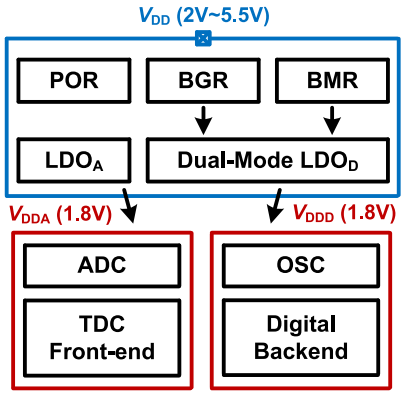


Fig. 6. Block diagram of the proposed TDC architecture organized by power domains.

integrated oscillators provide independent clock sources for core operations and digital communication, enabling precise timing control in the standby state.

Because many sensing systems typically operate intermittently—briefly activating for temperature conversions followed by a prolonged standby—minimizing standby current is essential for energy-efficient operation [23]. To this end, the proposed TDC integrates a dual-mode LDO (Dual-Mode LDO_D), which includes a bandgap reference (BGR), a main error amplifier (EA_{MAIN}), a low-power beta-multiplier reference (BMR), and a suberror amplifier (EA_{SUB}). During normal operation, the BGR and EA_{MAIN} provide precise voltage regulation; in standby, only the BMR and EA_{SUB} remain active while the analog front-end and nonessential digital blocks are powered down. As a result, the chip-level standby current is as low as 420 nA at 2.0 V.

This selective power management scheme, enabled by fully integrated low-power References and regulators, substantially improves energy efficiency and makes the architecture well-suited to systems with intermittent activity.

IV. Implementation of Proposed TDC

A. Overall Main Signal Path Architecture

The proposed TDC comprises three main signal-path components: a single-BJT-based front-end circuit, a switched-capacitor incremental delta-sigma modulator (I-ΔΣ ADC), and a digital backend. Fig. 7 shows the front-end circuitry, comprising a bias circuit and a BJT core circuit.

To avoid mismatch errors commonly encountered in dual-BJT designs, the core circuit employs a single-BJT Q_{CORE} sequentially biased at $5 \cdot I_B$ and $25 \cdot I_B$.

Fig. 8 details the I-ΔΣ ADC. It digitizes the ratio $k \cdot (\Delta V_{BE}/V_{BE})$, where the scaling factor k is 4. The on-chip digital backend processes the resulting digital code to compute the final temperature output in degrees Celsius as follows:

$$D_{OUT} = A \cdot \mu + B \tag{11}$$

where $A \approx 681$ and $B \approx -295$ are calibration constants obtained through batch-level calibration and stored in e-fuse memory.

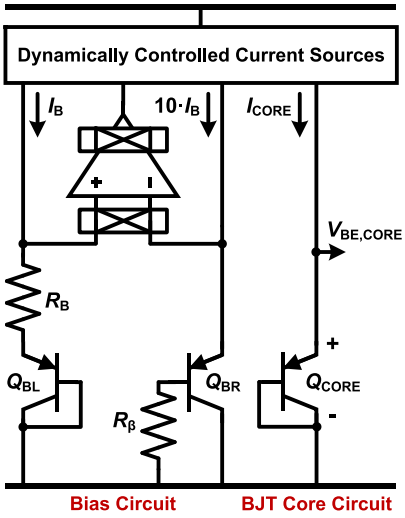


Fig. 7. Circuit diagram of the proposed TDC front-end.

B. Precision Techniques

The overall accuracy is primarily limited by a mismatch in the front-end current sources. To suppress this error, DEM rotates unit current segments so that device-to-device variations are averaged in time [14]. The DEM update rate is chosen sufficiently high with respect to the conversion bandwidth so that any residual tones are shaped out of band.

Another critical source of inaccuracy arises from the spread of the BJT current gain (β) across PVT. Such variations directly impact the V_{BE}, expressed by the fundamental BJT relationship as follows:

$$V_{BE} = \frac{kT}{q} \cdot \ln\left(\frac{I_{BIAS}}{I_S} \cdot \frac{\beta}{\beta+1}\right) \tag{12}$$

which emphasizes the increased sensitivity at low β, typical of modern CMOS [13]. To desensitize V_{BE} to β, the bias circuit incorporates a β-compensation resistor R_β (set to $R_\beta/10$ in this design), which counteracts the influence of current gain on the bias current, thereby stabilizing the resulting V_{BE} [15].

Accuracy is further affected by finite op-amp gain and low-frequency noise in the bias amplifier [20]. A self-biased folded-cascode operational amplifier with a DC gain exceeding 90 dB is employed to minimize these errors. To mitigate flicker noise and offset, chopping is applied to the bias amplifier; the chopping frequency is set to $F_{CP} = F_S/32 = 50/32$ kHz = 1.5625 kHz. The chopping frequency F_{CP} is strategically selected as $F_S/32 = 50/32$ kHz, which is below the I-ΔΣ modulator's sampling frequency $F_S = 50$ kHz yet above the flicker corner of the bias circuitry, ensuring effective modulation and subsequent suppression of low-frequency errors [14].

C. Readout Topology

As shown in Fig. 8, digitization is performed by a second-order switched-capacitor I-ΔΣ modulator with a cascade-of-integrators-with-distributed-feedback (CIFB) architecture, followed by an on-chip third-order sinc decimation filter. The ADC directly digitizes the ratio of the two front-end voltages, V_{BE} and ΔV_{BE}. The filter's oversampling clock cycles are

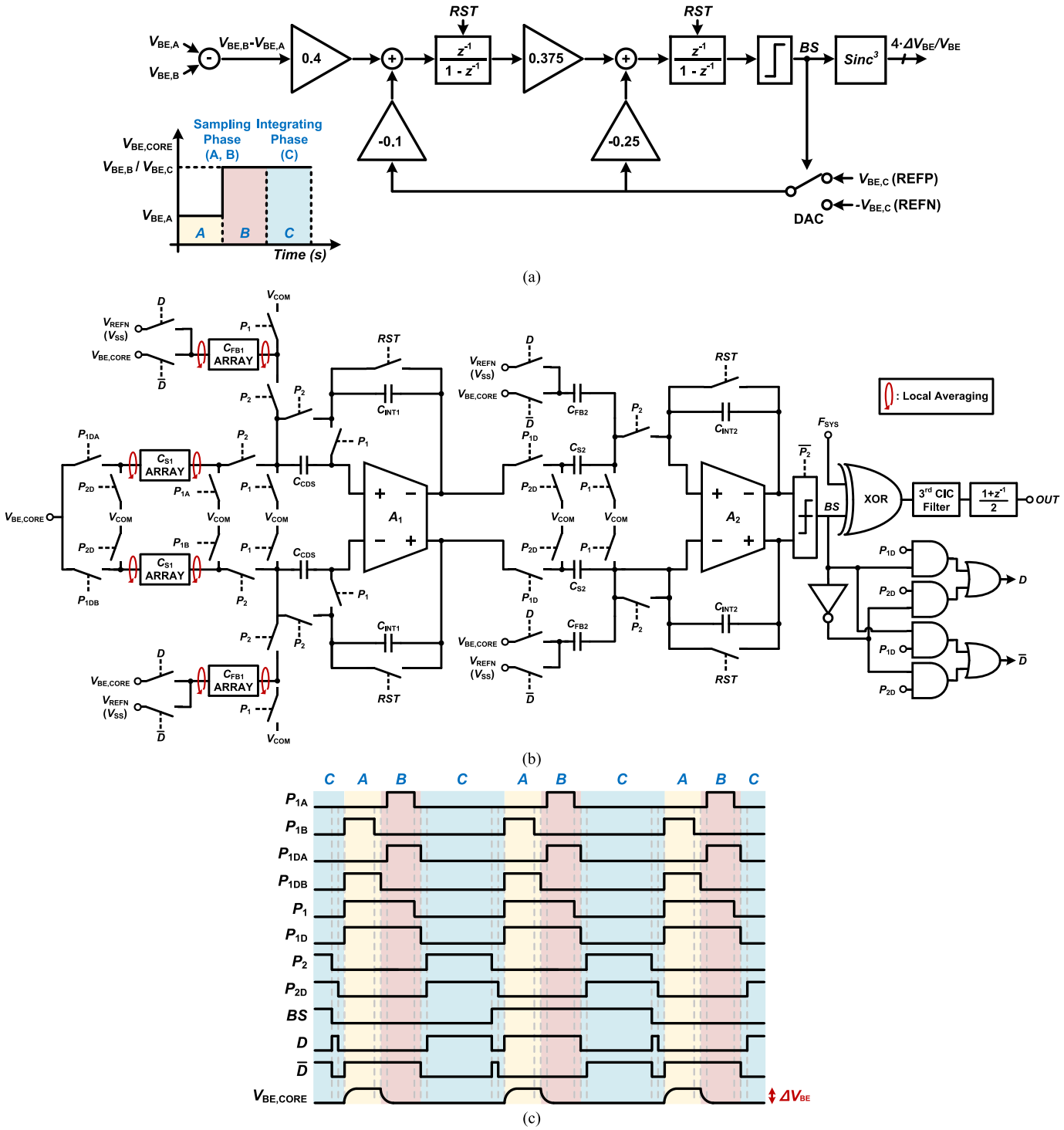


Fig. 8. (a) Timing diagram of the proposed I-ΔΣ readout. (b) Circuit implementation of the I-ΔΣ. (c) Its timing diagram.

configurable among 192, 384, 768, 1536, or 3072 cycles, with a conversion time of 7.68 ms for 384 oversampling cycles. The oversampling clock frequency of the ΔΣ modulator is 50 kHz, and the integrators are reset after each conversion, as strobed by the decimation filter output, ensuring accurate and stable digitization over successive conversion cycles.

Fig. 8(a) summarizes the timing diagram of the proposed I-ΔΣ readout. During phases A and B, the ΔΣ modulator samples $V_{BE,A}$ and $V_{BE,B}$ such that $\Delta V_{BE} = V_{BE,B}$-$V_{BE,A}$, while in phase C, the sampled $V_{BE,C}$ is applied as the ADC reference. With the first-integrator gain set by $C_{S1}/C_{FB1} = 0.4/0.1 = 4$, the resulting conversion target becomes

$$OUT = \frac{C_{S1}}{C_{FB1}} \cdot \frac{V_{BE,B} - V_{BE,A}}{V_{BE,C}} = 4 \cdot \frac{\Delta V_{BE}}{V_{BE}}. \quad (13)$$

As shown in Fig. 8(b) and (c), the $V_{BE,CORE}$ voltage, synchronized with the P_{1DB} timing signal, is connected to

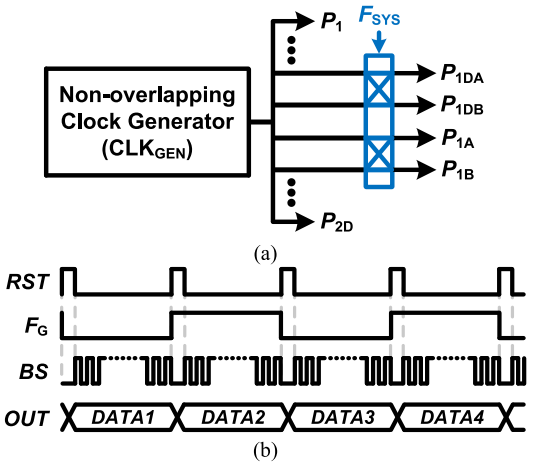


Fig. 9. (a) Proposed clock-based system-level chopping technique. (b) Its corresponding timing diagram.

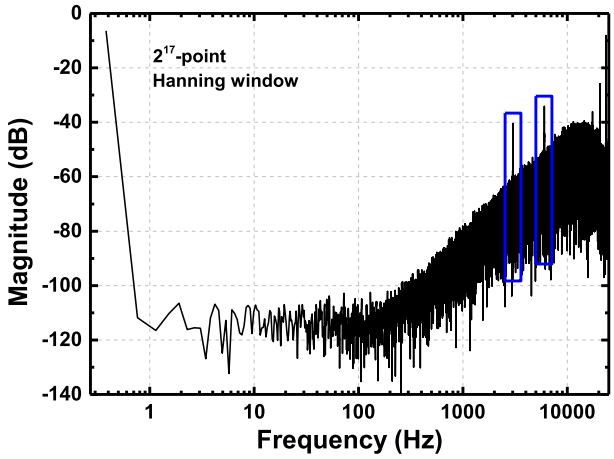


Fig. 10. Simulated power spectrum of the ΔΣ modulator bitstream at room temperature.

the REFP, INP, and INN nodes of the ADC, ensuring a precise timing alignment. The timing diagram in Fig. 8(c) further details this operation, illustrating the distinct intervals A, B, and C that directly correspond to the sequential biasing scheme introduced in Figs. 5(a) and 8(a). During the sampling phase of the first integrator (Phases A and B), the front-end voltages corresponding to two sequentially applied bias currents—$5 \cdot I_B$ (Phase A) and $25 \cdot I_B$ (Phase B)—are captured using nonoverlapping clock signals P_{1A}, P_{1B}, P_{1DA}, and P_{1DB}. To minimize charge injection and clock feedthrough effects, a bottom-plate sampling is employed [24]. Subsequently, in the integration phase (Phase C), the sampled V_{BE} voltage corresponding to the $25 \cdot I_B$ current level is utilized as the REFP of the ADC for the integration.

The first integrator is implemented using independently configured capacitor arrays; specifically, a C_{S1} array consisting of 16 unit capacitors and a C_{FB1} array composed of 4 unit capacitors. A local averaging technique is applied to these capacitors to mitigate mismatch-induced errors. A swapping DAC topology is utilized, reducing the impact of reference-induced noise [25]. Additionally, CDS using C_{CDS} is applied to the first integrator to effectively suppress offset and flicker noise of the integrator's amplifier [26].

Fig. 9 presents the proposed clock-based system-level chopping technique. Two dedicated choppers are placed between the nonoverlapping clock generator and the sampling clocks: one between P_{1A} and P_{1B}, and another between P_{1DA} and P_{1DB}. These choppers invert the polarity of the sampled ΔV_{BE} under the control signal F_{SYS}, periodically modulating the input. An XOR stage after the comparator demodulates the signal, which is then low-pass filtered by a digital FIR filter to suppress residual offset.

Fig. 10 shows the postlayout simulated power spectrum of the second-order ΔΣ modulator bitstream at room temperature. Since the internal decimation filter fully integrates and resets the ADC's integrators after each conversion, the modulator's raw bitstream is not accessible externally, and thus, a simulated spectrum is shown. Periodic tones from DEM averaging and chopping are visible but removed by the on-chip decimation filter. From transient noise simulations with a DC input, the ADC achieves an effective resolution (ER) of 16.7 bits, which is equivalent to ENOB in the DC domain.

D. Power Management

In this design, the standby state is achieved by turning off most internal circuit blocks. In contrast, only the power-on-reset (POR) circuit and the essential digital logic remain active, powered by an internal LDO. To eliminate the need for external output capacitors and reduce package complexity, a capacitor-less LDO structure is employed.

Fig. 11(a) illustrates the proposed dual-mode LDO_D architecture, and Fig. 11(b) shows the corresponding enable timing diagram during state transitions. Since the performance requirements—such as transient response and load current demand—differ between the normal and standby states, the LDO employs two dedicated error amplifiers, one optimized for each state. Specifically, the EA_{MAIN} is activated during normal operation, whereas the EA_{SUB} is used during the standby state. To enhance loop stability during normal operation, a static current source I_{BLEED} is activated only when EA_{MAIN} is enabled.

The EA_{SUB} is implemented using a minimal 5-transistor structure that consumes only 19 nA and has an inherently slow transient response. As a result, during the transition to standby, the gate voltage of PM2 settles slowly, resulting in a temporary voltage drop at the logic supply node.

To mitigate this issue, the proposed architecture introduces an intermediate transition state in which the switch SW_{PASS} is activated, thereby pre-setting the gate voltage of transistor PM_2 before disabling EA_{MAIN}. Fig. 12 illustrates the simulated transient response of the Dual-Mode LDO_D during this state transition. As shown in the top waveforms, without SW_{PASS}, the slow settling of the EA_{SUB} results in a gradual change in $V_{PG,SUB}$, causing a significant voltage drop in $V_{LDO,OUT}$ that could compromise digital logic integrity. In contrast, the bottom waveforms show that with SW_{PASS} activated during the transition, the voltage drop is effectively suppressed. This ensures the digital logic voltage is consistently maintained,

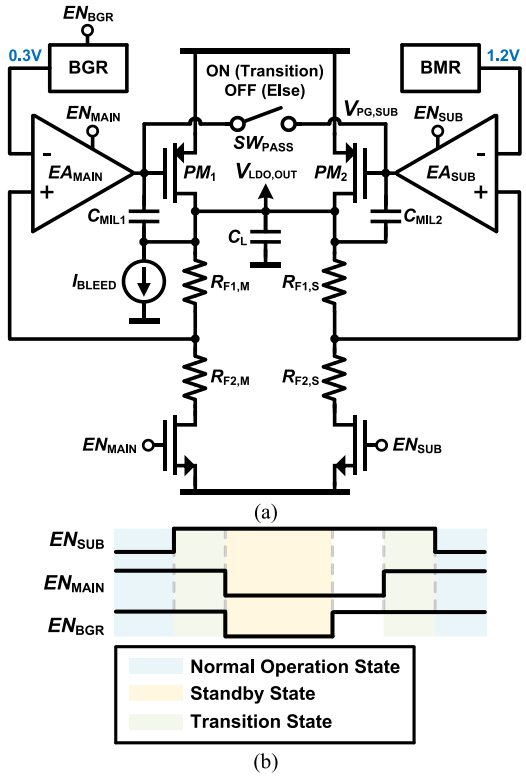


Fig. 11. (a) Proposed dual-mode capacitor-less LDO_D structure designed for digital logic operation in the standby state. (b) It's enable-signal timing.

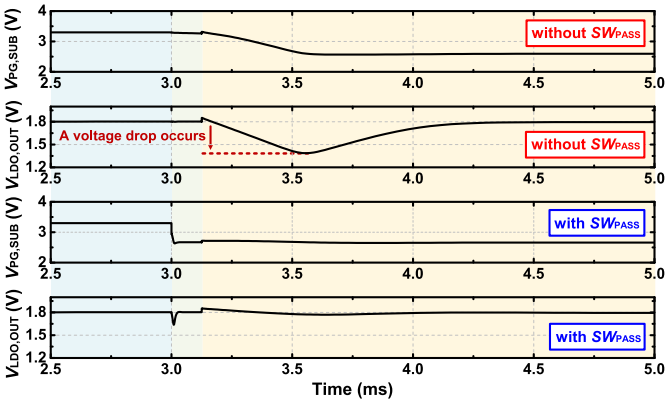


Fig. 12. Simulated waveforms of the dual-mode LDO_D comparing mode transitions with and without SW_{PASS}.

enabling robust transitions between normal operation and standby states. The transition state inherently corresponds to a minimal-load condition, as most internal circuits are turned off during mode switching. To ensure that the gate voltages required for PM_1 and PM_2—under minimal-load conditions in normal and standby states, respectively—are identical, the transistor size ratio is set equal to the resistor divider ratio, i.e., $(R_{F1,S} + R_{F2,S}):(R_{F1,M} + R_{F2,M}) = 30:1$.

Through this method, the digital logic voltage is consistently maintained during standby, while all unnecessary circuit blocks remain inactive. The transition from standby state to normal operation follows a sequential enablement process: initially activating the BGR ($EN_{BGR} = 1$), then transitioning

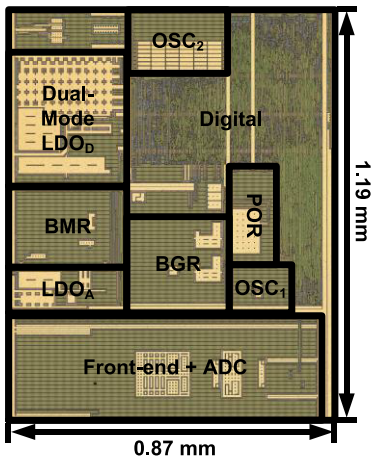


Fig. 13. Chip micrograph.

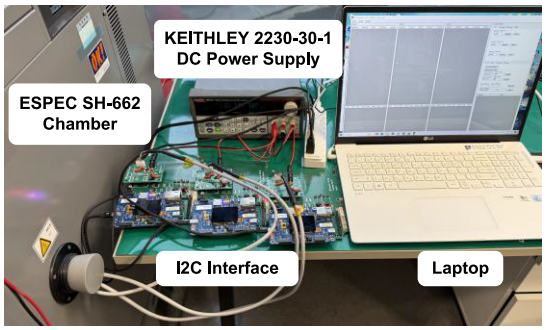
through an intermediate state, and finally disabling the EA_{SUB} ($EN_{SUB} = 0$). This carefully orchestrated sequencing ensures smooth and stable transitions between states, thereby preserving overall system reliability.

V. Experimental Results

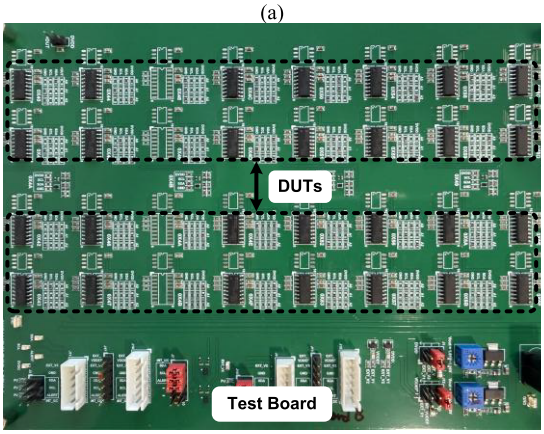
The proposed fully integrated single-BJT-based TDC was fabricated in a standard 0.18 μm CMOS process, occupying a total active area of 1.03 mm^2, of which the sensor front-end and ADC core account for 0.15 mm^2. The chip micrograph is shown in Fig. 13. The TDC integrates all necessary blocks, including the sensing front-end, I-$\Delta\Sigma$ ADC, power management circuitry, oscillators, embedded e-fuse memory, essential digital logic, and an I^2C-compatible interface.

As shown in Fig. 14(a), the experimental setup incorporates a thermal chamber (ESPEC SH-662) that houses the test board with the devices under test (DUTs), as depicted in Fig. 14(b). Since most of the necessary peripheral circuits are integrated within the chip, minimal external equipment or components are required. The KEITHLEY 2230-30-1 DC power supply directly provides the supply voltage to the test board, while a laptop controls both the chamber and the power supply to enable automated temperature and supply voltage sweeps and communicates with the chip via an I2C interface. To ensure adequate temperature settling within the chamber, each temperature step is maintained for over 4 h, and the chamber fan is deactivated for 3 min prior to data recording to minimize any potential airflow-induced effects.

The temperature inaccuracy was characterized using 18 samples from −40 °C to 125 °C in a thermal chamber with a constant supply voltage of 3.3 V. For the characterization, the calibration parameters from (6) and (11) were set to $\alpha/k = 3.77$, $A = 680.64$, and $B = -294.54$. Without trimming, the measured temperature inaccuracy was ±1.2 °C, as shown in Fig. 15(a). After applying a single-point trim at 30 °C, the inaccuracy improved to ±0.23 °C, as depicted in Fig. 15(b). This accuracy accounts for various sources of error, including residual V_{BE} spread and ADC gain factor (k) variations in the TDC front-end and ADC, as well as errors introduced by the on-chip LDOs, oscillators, and other digital logic. This



(a)



(b)

Fig. 14. (a) Measurement setup. (b) Test board with the DUTs, which is placed inside the chamber.

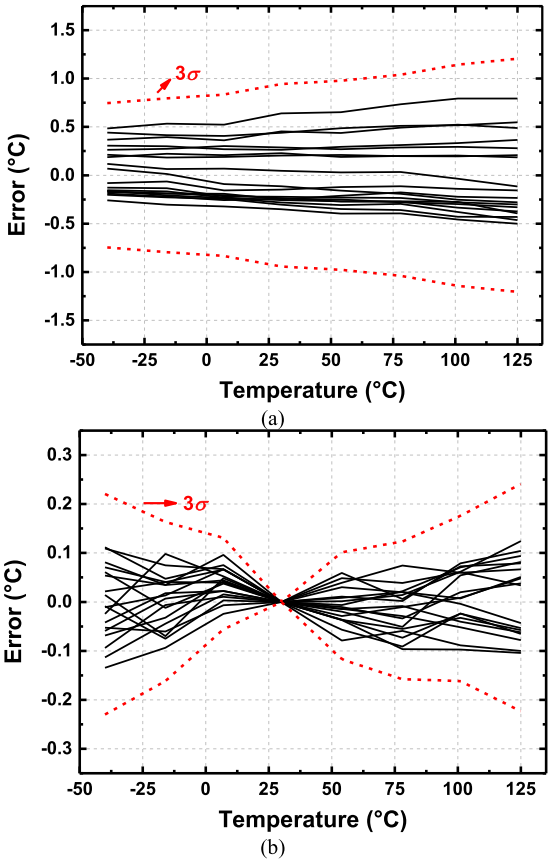


Fig. 15. (a) Measured temperature error across 18 single-BJT-based TDCs without trimming. (b) Corresponding results after applying one-point calibration. Dashed lines denote the ±3σ error margins.

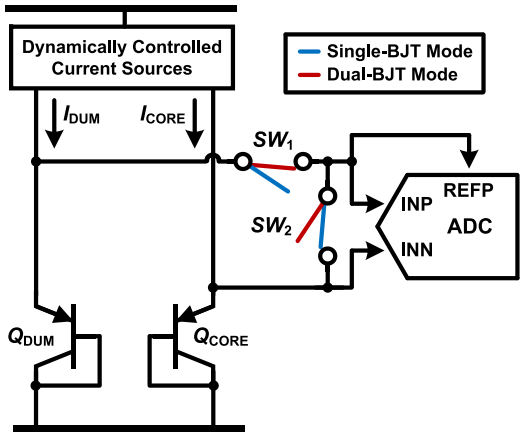


Fig. 16. Simplified architecture of the TDC configurable for single-BJT or dual-BJT operation for testing.

result indicates that the TDC maintains high performance in a compact, fully integrated system comprising all critical analog and digital components.

For a direct comparison, a dual-BJT-based architecture was co-integrated on the same chip, as shown in Fig. 16. While the ADC structure remained unchanged, the front-end was reconfigurable using switches SW_1 and SW_2 to enable operation with either the single-BJT or dual-BJT configuration. In the dual-BJT configuration, the core current (I_{CORE}) and dummy current (I_{DUM}) were fixed at $5 \cdot I_B$ and $25 \cdot I_B$, respectively, maintaining the same DEM scheme. For the dual-BJT configuration, without trimming, the measured inaccuracy was ±1.46 °C, as shown in Fig. 17(a). After applying the same single-point calibration, the inaccuracy improved to ±0.37 °C, as depicted in Fig. 17(b). This result demonstrates the clear performance advantage of the proposed single-BJT-based design.

The ADC resolution at room temperature was evaluated across various conversion times of 3.84, 7.68, 15.36, 30.72, and 61.44 ms, as shown in Fig. 18. The default conversion time was 7.68 ms to ensure kT/C-limited operation, achieving a resolution of 6.71 mK at room temperature.

Fig. 19 presents the measured average temperature error across −40 °C to 125 °C under various supply voltages of 2.0, 3.3, and 5.5 V. The minimized error at 3.3 V is attributed to the one-point calibration being performed at this nominal voltage. The results demonstrate that the proposed TDC maintains stable and accurate temperature sensing over the 2.0–5.5 V supply range. The supply sensitivity, quantified as the average error variation across the entire temperature range, is only 2.54 m°C/V, underscoring the robust and supply-invariant performance of the fully integrated design. This confirms the effectiveness of the implemented power management circuits and their capability to maintain accuracy despite supply voltage fluctuations.

Fig. 20 presents the measured current consumption in the standby state at room temperature. The standby current ranges from 420 nA at the minimum supply voltage to 760 nA at

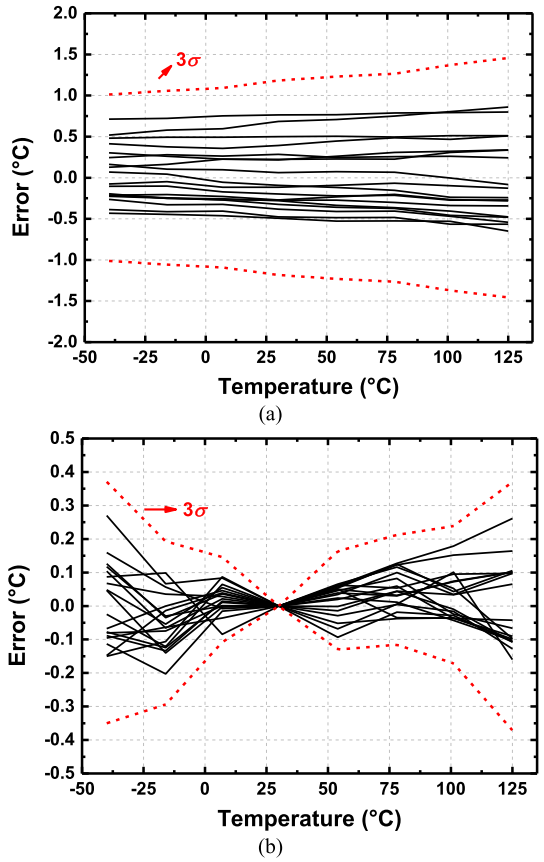


Fig. 17. (a) Measured temperature error across 18 dual-BJT-based TDCs without trimming. (b) Corresponding results after applying one-point calibration. Dashed lines denote the $\pm 3\sigma$ error margins.

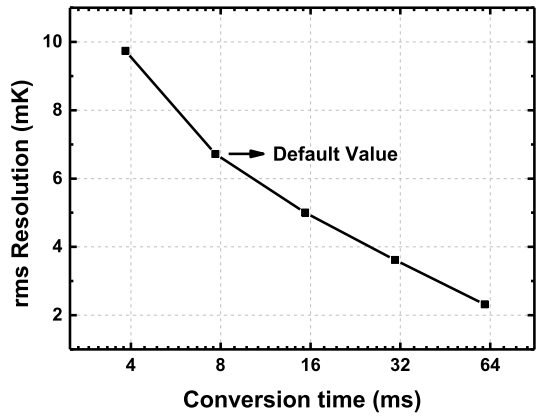


Fig. 18. Measured rms resolution versus ADC conversion time at room temperature.

the maximum. This corresponds to a 99.3% reduction relative to the normal-mode operation current of 66 μA measured at 3.3 V.

Fig. 21 illustrates the power breakdown in the standby and normal operation states under a 3.3 V supply. In the standby state, the static current is dominated by three primary blocks: the BMR, the POR, and the dual-mode LDO_D. Within the total normal operation state current, the sensor core, which includes the sensor front-end and the ADC, consumes 18.9 μA.

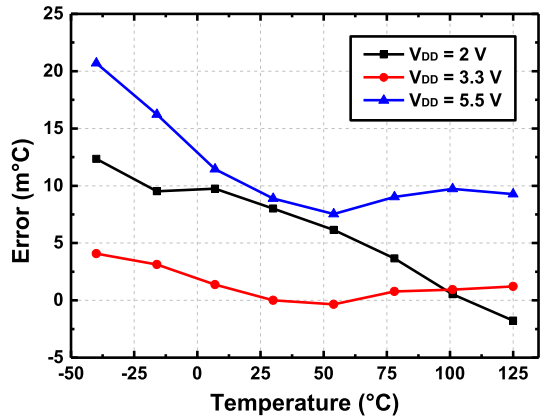


Fig. 19. Measured average temperature error across temperature for different supply voltages.

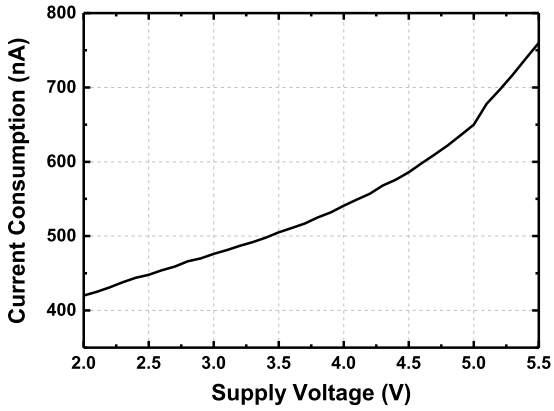


Fig. 20. Measured current consumption of the TDC in the standby state versus supply voltage.

TABLE I
AVERAGE CURRENT CONSUMPTION ACCORDING TO DIFFERENT USAGE SCENARIOS

Conversion Period (ms)	27.5	55	110	220
Average Current Consumption (μA)	18.8	9.6	5.1	2.8

This core consumption is supplied from a 1.8 V internal rail. Based on this core power and the 7.68 ms conversion time, the resolution figure-of-merit (FoM) of 11.8 pJ $\cdot$ K^2.

To demonstrate the energy efficiency in practical duty-cycled applications, the average current consumption was evaluated with respect to various conversion periods. These periods are implemented as digitally configurable options, allowing users to select the optimal duty cycle for their specific usage scenarios. Table I lists the average current consumption according to different usage scenarios. As the conversion period increases, the average current consumption significantly decreases, approaching the standby current level. This indicates that the proposed TDC is well-suited for long-term monitoring applications where the device spends the majority of its time in the standby state.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	[3]	[6]	[14]	[16]	[20]	[27]	[28]	**This Work**	
Technology	180 nm CMOS	160 nm CMOS	180 nm CMOS	130 nm CMOS	130 nm CMOS	110 nm CMOS	180 nm CMOS	**180 nm CMOS**	
On-Chip Components	Front-end +ADC	Front-end +ADC	Front-end +ADC	Front-end +ADC	Front-end +ADC	Front-end +ADC	Front-end +ADC	**Fully integrated**	**Front-end +ADC**
Supply voltage (V)	1.8	1.8	1.5-2	1.8	2-3.6	2.97-3.63	1.8	**2.0-5.5**	**1.8**
Supply Sensitivity (m°C/V)	230	-	440	-	50	-	-	**2.54**	
Sensor type	NPN	PNP	PNP	MOS	PNP	TSD	NPN	**PNP**	
Number of Sensing Elements Used *	2	2	2	1	2	1	2	**1**	
Architecture	NS-SAR	ΔΣ	ΔΣ	ΔΣ	ΔΣ	ΔΣ	OS-SAR	**ΔΣ**	
Chip area (mm^2)	0.057	0.15	0.42	0.63	0.29	0.26	0.08	**1.03**	**0.15**
Supply current (μA)	34	5.4	2.5	13.1	95	985	22	**66 (0.42) ****	**18.9**
Temperature Range (°C)	-50 to 110	-40 to 180	-50 to 180	-40 to 90	-40 to 125	-40 to 125	-20 to 80	**-40 to 125**	
3σ Inaccuracy	1.96%	± 0.2 °C (1-p cal)	± 0.39 °C (1-p cal)	+0.75 °C / -0.92 °C (1-p cal)	± 0.47 °C (1-p cal)	± 7.3 °C (0-p cal)	1.77%	**± 0.23 °C (1-p cal)**	
Resolution (mK)	92	23	17.6	40	16	700	158	**6.71**	
Conversion Time (ms)	0.08	20	8.3	6.4	5.12	0.4	0.064	**7.68**	
Resolution FoM (nJ·K^2) ***	$4.10\cdot10^{-2}$	$1.03\cdot10^{-1}$	$9.7\cdot10^{-3}$	$2.53\cdot10^{-1}$	$4.11\cdot10^{-1}$	$6.37\cdot10^{2}$	$6.30\cdot10^{-2}$	**$7.55\cdot10^{-2}$**	**$1.18\cdot10^{-2}$**

* Counts sensing elements used solely for PTAT generation; excludes auxiliary devices.
** All blocks including the front-end and ADC are included. Value in parentheses indicates the current in standby state.
*** Resolution FoM = Energy/Conversion×Resolution^2.

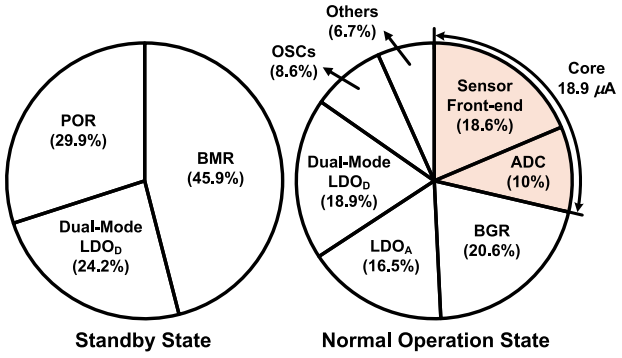


Fig. 21. Power breakdown in standby and normal operation states.

Finally, Table II summarizes the performance comparison between the proposed fully integrated TDC and recent state-of-the-art BJT-based designs. For this work, the left column corresponds to the fully integrated configuration, while the right column pertains only to the front-end and ADC. The TDC exhibits high accuracy, robust integration, and superior system-level characteristics. Unlike conventional BJT-based designs that require multiple matched BJTs to generate ΔV_{BE}, the proposed architecture employs only a single BJT, highlighting its simplicity and mismatch-immune operation. In addition, it is the only design among the compared works that fully integrates all required analog and digital subsystems on a single chip. The architecture uniquely supports a wide 2.0–5.5 V supply range with exceptionally low supply sensitivity of 2.54 m°C/V. Despite the challenges of on-chip integration, such as variations in oscillator output frequency and LDO output voltage across process, voltage, and temperature conditions, which make achieving consistent performance significantly more difficult than in designs relying on external components, the TDC achieves ±0.23 °C (3σ) accuracy with a single-point calibration. Furthermore, the standby state current is reduced to 420 nA, demonstrating outstanding energy efficiency.

VI. CONCLUSION

This article presents a fully integrated single-BJT-based TDC, fabricated in a standard 0.18 μm CMOS process. By sequentially biasing a single-BJT, the architecture eliminates mismatch between distinct BJTs, thereby enabling ΔV_{BE} generation that is immune to device mismatch and improving

accuracy without the need for additional complex trimming techniques. The fully integrated implementation incorporates all required analog and digital subsystems to ensure standalone operation and robust performance across a wide 2.0–5.5 V supply range. The chip achieves a measured inaccuracy of ± 0.23 °C (3σ) across −40 °C to 125 °C with a single-point calibration, and attains a resolution FoM of 11.8 pJ · K^2 at a 7.68 ms conversion time. In addition, the integrated dual-mode power management scheme enables a low standby current of 420 nA, ensuring energy-efficient duty-cycled operation. These results collectively demonstrate that the TDC offers a robust and compact solution for high-accuracy and low-power temperature sensing in intermittently active platforms, while maintaining operation over 2.0–5.5 V with a measured supply sensitivity of 2.54 m°C/V and showing superior posttrim accuracy compared with a dual-BJT counterpart.

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