# An Ultrasonic Sensor IC for Automotive Parking Assist with Module ID Detection

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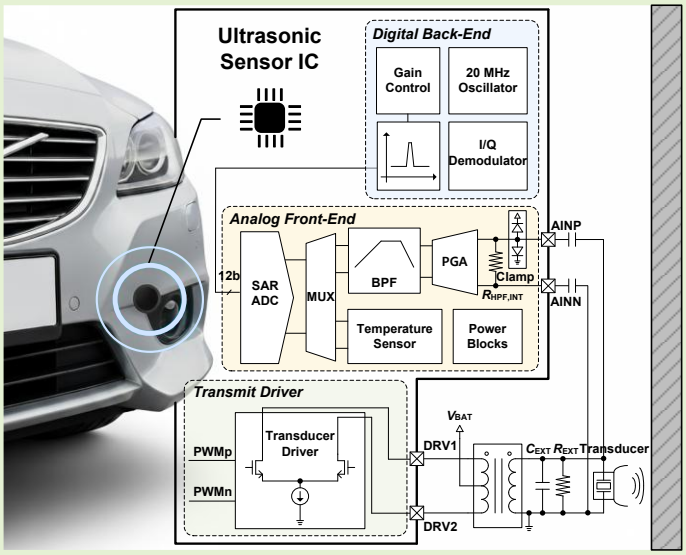
***Abstract*— This paper presents an integrated circuit (IC) for automotive parking assistance, which performs ultrasonic time-of-flight (ToF) ranging and module identification. The IC integrates a bidirectional transducer driver for a center-tapped transformer, a low-noise high-gain analog front-end (AFE) with programmable gain and band-pass filtering, a 12-bit successive-approximation register analog-digital converter, and a digital back-end for envelope extraction and ID detection based on π/4-differential quadrature phase shift keying (DQPSK). To cope with severe acoustic echo attenuation over long distances, the receive path provides up to 108 dB system gain while maintaining adequate bandwidth around the 58-kHz ultrasonic transducer resonance frequency. Fabricated in 130-nm CMOS, the IC operates directly from a 12-V automotive battery, occupies 14.43 mm$^2$, and dissipates 399.7 mW, excluding the transducer driver current. The IC also supports ID detection for various sensor modules. Measurements in an anechoic chamber demonstrate a detectable range of 0.25–9.8 m in normal mode and experimentally verify 10-cm detection in the indirect mode, while geometric path analysis indicates a 2-cm theoretical limit. The measured distance error is 2.51 mm$_{rms}$ at an object distance of 1 m. These results confirm the practicality of the proposed IC for long-range, ID-aware ultrasonic parking-assistance systems.**




***Index Terms*— Analog front-end (AFE); differential quadrature phase shift keying (DQPSK); distance detection; parking assist system; programmable-gain amplifier (PGA); time-of-flight (ToF); ultrasonic transducer**

## I. Introduction

INTEGRATION of sensing and signal-processing technologies has markedly improved vehicle safety and driver convenience. Conventional parking-assist sensors typically cover a range of about 3 m, which suffices for low-speed maneuvers but is inadequate for features such as advanced driver-assistance systems (ADAS), rear-collision avoidance, and remote smart parking that require longer detection distances [1]–[4]. To satisfy these demands, it is necessary to employ sensor readout ICs (ROICs) that offer high system gain, carefully shaped analog bandwidth, and robust noise performance.

Distance sensing in automotive applications has been implemented using ultrasonic, infrared, light detection and ranging (LiDAR), radio detection and ranging (RADAR), and

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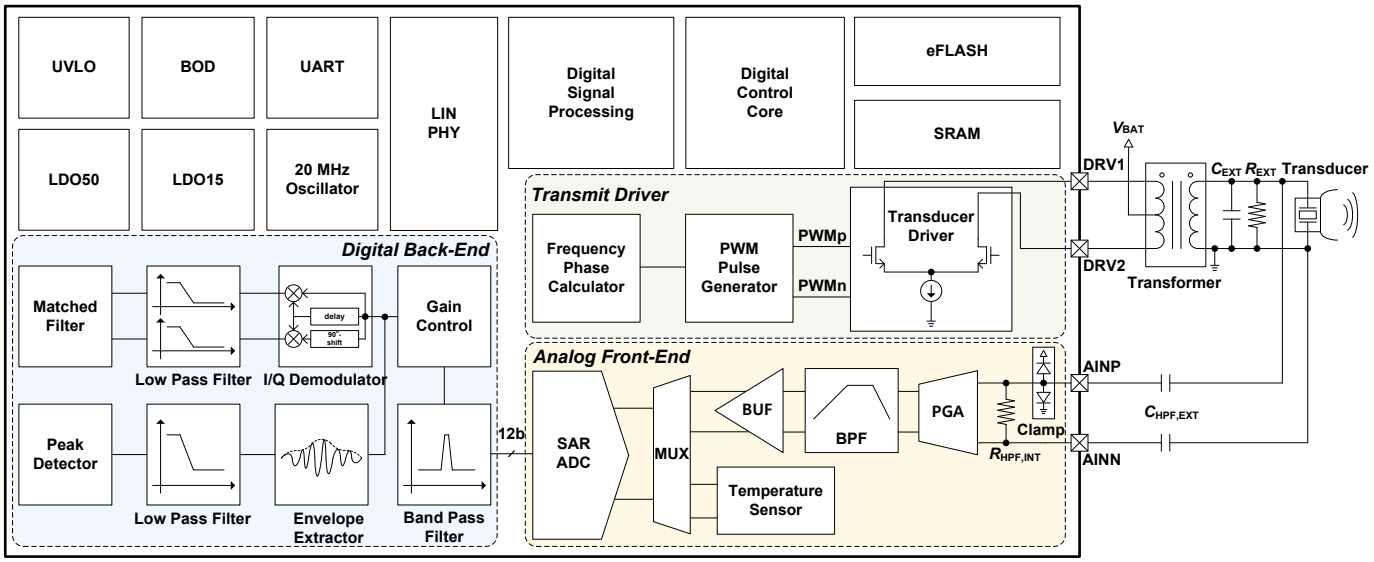



Fig. 1. Overall architecture of the proposed ultrasonic sensor module.

stereo-vision sensors, each offering distinct trade-offs between cost and performance [5]. Among these technologies, ultrasonic transducers are attractive for short- to mid-range detection in adverse weather conditions, owing to their maturity and ease of system integration [6]. Ultrasonic front-ends are typically driven either directly or via a transformer. Although direct driving offers simplicity, it often fails to provide the sufficient excitation amplitude required for mid-range automotive applications. Therefore, a center-tapped transformer drive is adopted to boost the effective transducer voltage, thereby enhancing echo returns. In addition, passive components are connected in parallel with the transformer to shorten the transducer ring-down time, improving close-range detectability [7].

While our preliminary work was limited to the circuit-level evaluation of a high-gain analog front-end (AFE) [8], this paper extends the research to address a systemic limitation in conventional automotive ultrasonic ranging ICs. A conventional receiver estimates object distance based on the envelope or arrival time of an echo, but inherently lacks the capability to verify the origin of the acoustic waveform. This limitation can lead to ambiguous detections when multiple ultrasonic modules operate within overlapping acoustic fields.

To address this, this work presents a monolithic module-selective ultrasonic sensor IC. The principal contribution is the implementation of a dual-purpose receive architecture that extracts both time-of-flight (ToF) and transmitter-associated ID information from a single received waveform. Instead of duplicating analog channels, the IC utilizes a single protected AFE and a 12-bit SAR ADC. The digitized output is concurrently processed by a bifurcated digital back-end (DBE) performing envelope-based ToF extraction and π/4-differential quadrature phase shift keying (DQPSK)-based module identification.

This architecture is explicitly co-designed with the electro-acoustic constraints of piezoelectric transducers. Conventional binary PSK (BPSK) or quadrature PSK (QPSK) transitions cross the origin (0V), inducing severe mechanical ring-down distortion. To resolve this, the system employs π/4-DQPSK, which limits phase transitions to {± π/4, ±3 π/4} to maintain a stable acoustic envelope, while halving the symbol rate to accommodate the narrow 2–3 kHz transducer bandwidth. Furthermore, a non-coherent delay-and-multiply demodulator eliminates the need for an explicit carrier-recovery phase-locked loop (PLL), and a resource-shared sequential multiply-accumulate (MAC) structure performs 124-sample correlation without extensive parallel multiplier arrays.

This work presents a monolithically integrated ultrasonic sensor IC designed for an automotive parking assistance system (PAS). The proposed IC incorporates a bidirectional transformer-driven transmitter, a low-noise AFE with a programmable-gain amplifier (PGA) and band-pass filtering, a 12-bit successive-approximation-register (SAR) ADC, and a DBE for envelope extraction and module identification using π/4-DQPSK. Fabricated in a 130-nm CMOS process, the IC operates directly from a 12-V battery, occupies 14.43 mm², and dissipates 399.7 mW excluding the driver current. Module-level measurements in an anechoic chamber demonstrate a detectable range of 0.25–9.8 m in the normal mode and experimentally verify 10-cm detection in the indirect mode, while geometric path analysis indicates a 2-cm theoretical limit. A ranging error of 2.51 $mm_{rms}$ is measured at an object distance of 1 m, confirming the effectiveness of the proposed approach for long-range, ID-aware PAS.

The remainder of this paper is organized as follows. Section II describes the overall system architecture. Section III details the transducer driver and AFE circuit implementations. Section IV presents the digital back-end. Section V reports the measurement setup and results. Section VI concludes the paper.

## II. Overall Architecture

Fig. 1 illustrates the architecture of the proposed ultrasonic distance-sensing module. The system consists of a transmit path comprising a current-mode transducer driver, a center-tapped transformer, and a bidirectional transducer, as well as a receive path comprising an AFE and a DBE. The driver generates two non-overlapping sink current pulses synchronized to the transducer's resonant frequency of 58 kHz. These currents

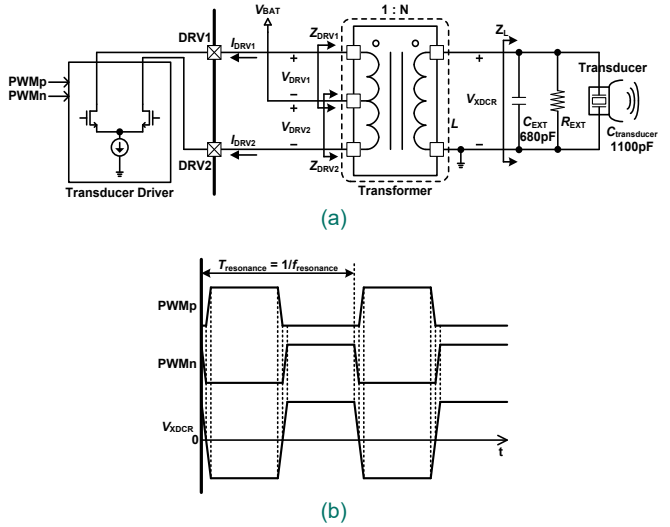



Fig. 2. (a) Simplified block diagram of ultrasonic transducer driver and transducer and (b) its timing diagram.

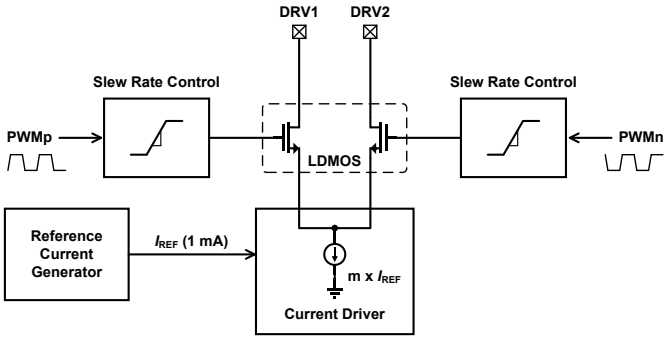



Fig. 3. Simplified block diagram of ultrasonic transducer driver.

generate a voltage across the transformer's primary winding, which is stepped up by the turns ratio to produce a differential excitation across the secondary winding for driving the transducer. This transformer-driven configuration effectively boosts the transducer excitation without requiring high-voltage devices.

Echoes reflected from a target are reconverted into an electrical signal at the transducer and subsequently processed by the receive chain. The AFE consists of an input clamp, a low-noise high-gain PGA, and a band-pass filter, followed by a 12-bit SAR ADC. The DBE performs band-pass filtering, envelope and peak detection, and in-phase and quadrature (I/Q) demodulation with matched filtering to extract ToF information and module identification based on π/4-DQPSK.

The IC integrates a transmit driver, AFE, DBE, on-chip power management, a temperature sensor, and a temperature-compensated 20-MHz relaxation oscillator. The power management block includes low-dropout regulators (LDOs) and protection features such as under-voltage lockout (UVLO) and brown-out detection (BOD). For communication and data exchange, the chip incorporates a local interconnect network physical layer (LIN-PHY) and a universal asynchronous receiver/transmitter (UART) interface for connection to a PC. To ensure reliable UART framing, the internal oscillator maintains a frequency accuracy within ±2.5% at the selected baud rate [9].

From a system perspective, long-range operation demands a high overall gain and a carefully shaped bandwidth centered on the 58-kHz resonance, while maintaining a low input-referred noise level. Since the PGA predominantly determines the AFE noise, its architecture is designed to achieve up to 60 dB of gain with a wide bandwidth [10].

## III. Analog Circuit Implementation

### A. Ultrasound Transducer Driver

Fig. 2(a) illustrates the block diagram of the ultrasonic transducer driver, the center-tapped transformer, and the bidirectional transducer. The proposed distance-sensing system employs a bidirectional piezoelectric transducer together with a push-pull, center-tapped transformer. The driver generates two non-overlapping sink currents ($I_{DRV1}$, $I_{DRV2}$) synchronized to the transducer's resonant frequency of 58 kHz, such that only one half of the primary is energized at a time. The transformer's center tap is connected to the automotive battery $V_{BAT}$ = 8–18 V, and laterally diffused MOS (LDMOS) transistors are used in the output stage to tolerate the high-voltage swing at the primary nodes.

The transducer can be modeled as an equivalent LC network. The resulting resonant frequency $f_{res}$ is expressed as follows:

$$f_{res} = \frac{1}{2\pi\sqrt{L(C_{transducer} + C_{EXT})}}, \quad (1)$$

where $L$ denotes the inductance of the transformer, $C_{transducer}$ represents the intrinsic capacitance of the transducer, and $C_{EXT}$ is an external capacitor of 680 pF, connected in parallel with the transducer. In this prototype, the external capacitor $C_{EXT}$ is chosen such that $f_{res}$ is set to 58 kHz.

Fig. 2(b) illustrates the timing diagram of the transducer driver, which generates differential, non-overlapping sink current pulses at a fixed frequency. A pulse-width modulation (PWM) generator controls the drive currents such that only one current source is active at a time.

When the upper half of the primary is driven, the fundamental AC voltage at node DRV1 can be expressed as follows:

$$V_{DRV1} = -I_{DRV1} \times Z_{DRV1}, \quad (2)$$

where $Z_{DRV1}$ denotes the equivalent impedance at node DRV1. $Z_{DRV1}$ is expressed as follows:

$$Z_{DRV1} = \frac{Z_L}{(2N)^2} = \frac{R_{EXT} \parallel \frac{1}{SC_{total}}}{(2N)^2}, \quad (3)$$

where $N$ is the ratio between the secondary winding and the primary winding, $Z_L$ is the load impedance, and $2N$ denotes the effective ratio from the half-primary to the secondary winding. The resulting secondary voltage $V_{XDCR,DRV1}$ due to $I_{DRV1}$ can be expressed as follows:

$$V_{XDCR,DRV1} = 2NV_{DRV1} = \frac{-I_{DRV1} \times Z_L}{2N}. \quad (4)$$

Similarly, excitation of the lower half of the primary

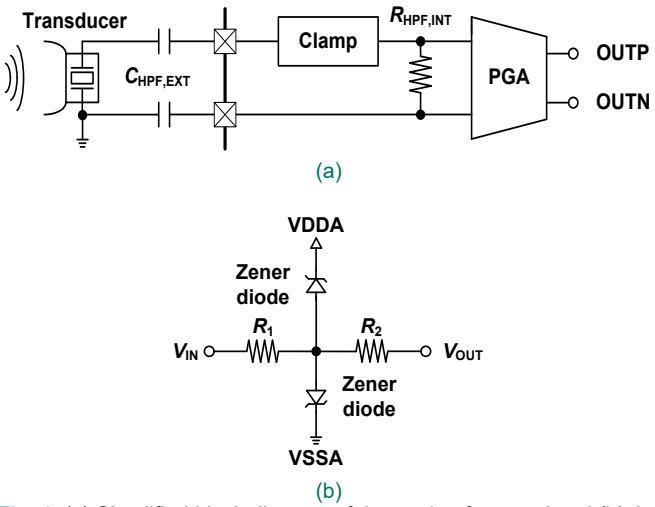



Fig. 4. (a) Simplified block diagram of the analog front-end and (b) the clamp circuit.

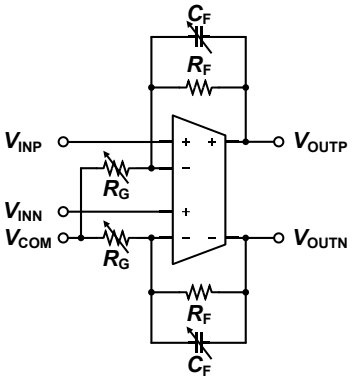



Fig. 5. Block diagram of the programmable gain amplifier.

produces

$$V_{\mathrm{XDCR,DRV2}} = \frac{I_{\mathrm{DRV2}} \times Z_{\mathrm{L}}}{2N}. \tag{5}$$

Hence, the voltage delivered to the transducer, $V_{\mathrm{XDCR}}$, which is the sum of $V_{\mathrm{XDCR,DRV1}}$ and $V_{\mathrm{XDCR,DRV2}}$, can be expressed as follows:

$$V_{\mathrm{XDCR}} = (I_{\mathrm{DRV2}} - I_{\mathrm{DRV1}}) \times \frac{Z_{\mathrm{L}}}{2N}, \tag{6}$$

which indicates that the excitation voltage is proportional to the instantaneous drive current.

Fig. 3 presents the block diagram of the ultrasonic transducer driver, which comprises a 1-mA reference, a programmable current multiplier, a slew-rate control circuit, and high-voltage pass transistors. The output current, derived from the 1-mA reference, is programmable in 63 discrete steps over a range of approximately 155 mA to 404 mA to accommodate various transducers and ranges. The current range and resolution are selected to ensure that the effective driving current remains adequately covered, even after accounting for the transformer and pass device series resistances. The slew-rate control shapes the switching edges to limit dV/dt at the primary nodes, mitigating ringing and electromagnetic interference. This is realized via a 3-bit programmable gate current control of the

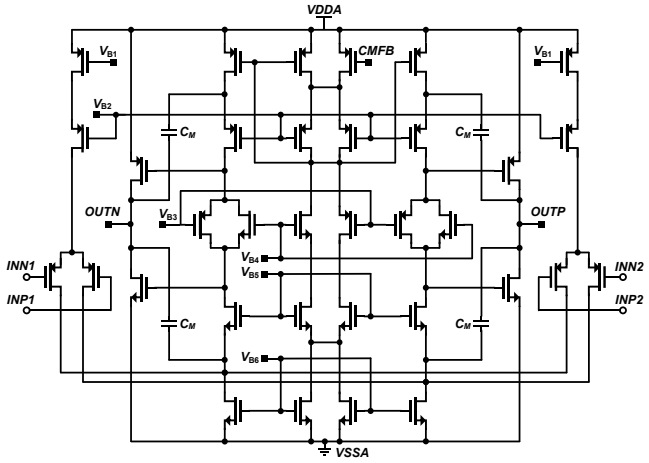



Fig. 6. Simplified schematic of DDA.

LDMOS pass transistors, adjusting the 10%-to-90% transition time from 0.1 µs to 1.4 µs. At a nominal 12-V supply, this yields an adjustable dV/dt range of 6.8 V/µs to 96 V/µs to accommodate various transducer loads.

### B. Programmable Gain Amplifier

Fig. 4(a) presents the block diagram of the transducer, clamp, high-pass filter (HPF), and PGA. In this shared-node transceiver architecture, the input voltage during near-field reflections or transducer ring-down can easily exceed 200 $V_{PP}$ depending on the selected transducer characteristics. For instance, the specific transducer utilized in the measurement setup generates voltage swings up to 140 $V_{PP}$. Because such massive swings would cause dielectric breakdown in standard on-chip capacitors, a high-voltage external AC-coupling capacitor is physically mandatory. Following this external coupling, a Zener-diode-based clamp circuit (Fig. 4(b)) confines the signal to the AFE supply range.

While area-efficient fully on-chip HPFs are prevalent in low-voltage applications, they are fundamentally unsuited for this design. The clamped rail-to-rail swings and high automotive temperatures would cause severe linearity degradation and cut-off frequency drift in active filters. Furthermore, achieving the 19.44 $\mu V_{rms}$ noise target constrains the equivalent noise resistance to 83.3 kΩ, which dictates a massive 470-pF capacitance to set the 4-kHz cut-off. Integrating this magnitude of capacitance would consume a prohibitive silicon area. Thus, the HPF utilizes external capacitors and internal resistors. A noninverting differential PGA with high input impedance is then adopted to minimize loading on this filter network.

Fig. 5 shows the block diagram of the PGA, which employs a differential difference amplifier (DDA) to process the two differential input pairs. The PGA gain is adjustable up to 60 dB in 6-dB steps by tuning a variable resistor $R_G$ and a fixed resistor $R_F$, while a variable capacitor $C_F$, is simultaneously adjusted to maintain a constant cutoff frequency across all gain settings. To enable these dynamic adjustments without any external hardware modifications, $R_G$ and $C_F$ are implemented as on-chip arrays governed by internal digital registers via the integrated UART/LIN interface.

Fig. 6. details the simplified schematic of the DDA employed in the PGA. To effectively amplify the highly attenuated

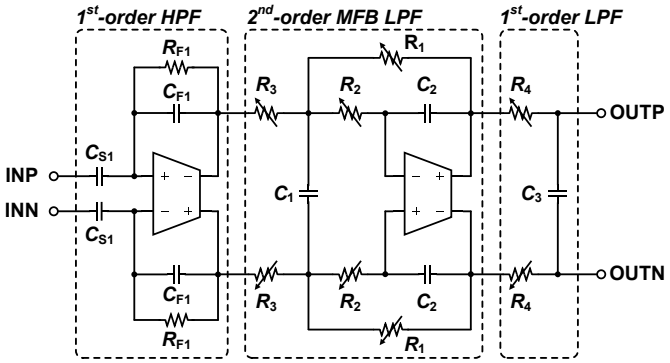



Fig. 7. Simplified schematic of the filters.

TABLE I
VALUES OF THE PASSIVE COMPONENTS USED IN FILTERS

| First-order HPF | | | Second-order MFB LPF | | | | | First-order LPF | |
|---|---|---|---|---|---|---|---|---|---|
| $C_S$ | $R_{F1}$ | $C_{F1}$ | $R_1$ | $R_2$ | $R_3$ | $C_1$ | $C_2$ | $R_4$ | $C_3$ |
| 10 pF | 15.9 MΩ | 10 pF | 949 kΩ | 456 kΩ | 130 kΩ | 5 pF | 150 fF | 400 kΩ | 350 fF |

ultrasonic echoes, the DDA utilizes a two-stage Class-AB topology that ensures a high open-loop gain and a wide output swing. Frequency compensation is appropriately applied to guarantee phase margin and loop stability across all programmable gain settings.

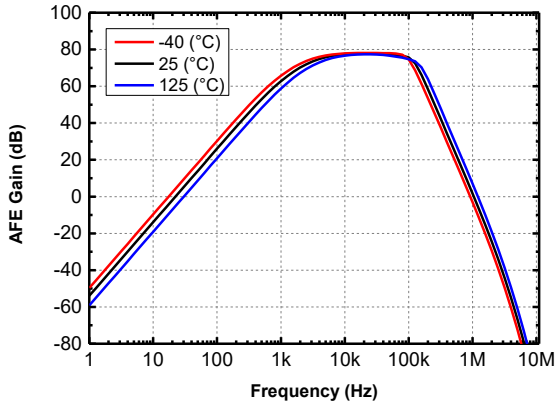
The input-referred noise of the PGA can be expressed as follows:

$$\overline{IRN_{\mathrm{PGA}}^2} = 4kTR_{\mathrm{G}} + \overline{IRN_{\mathrm{DDA}}^2} + 4kTR_{\mathrm{F}}\left(\frac{1}{G_{\mathrm{PGA}}}\right), \qquad (7)$$

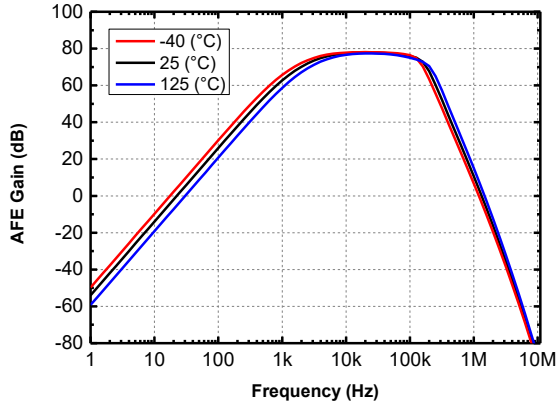
where $\overline{IRN_{\mathrm{DDA}}^2}$ is the input-referred noise of the DDA, and $G_{\mathrm{PGA}}$ is the gain of the PGA. As shown in (7), the thermal noise contribution from the feedback resistor becomes negligible owing to the high gain of the PGA. The input-referred noise of the DDA comprises both thermal noise and 1/*f* noise. To suppress the 1/*f* noise, PMOS transistors, which exhibit lower 1/*f* noise than NMOS devices, are employed in the input differential pairs. Post-layout noise simulations of the designed PMOS input pair–sized to satisfy the initial design target of 6.83 nV/√Hz at the maximum PGA gain of 60 dB–indicate a 1/f noise corner frequency of approximately 15 kHz. In contrast, an equivalently biased NMOS pair of the same transconductance in the adopted 130-nm process exhibits a 1/f corner exceeding 100 kHz. Because the 15-kHz PMOS corner lies below the 58-kHz transducer resonant frequency, the 1/f noise contribution at the signal band is minimized, enabling the amplifier to operate near its thermal noise floor.

### C. Filter Stages

The filter stages suppress out-of-band components, allowing only signals around the transducer resonant frequency to pass. Consequently, the AFE realizes an overall band-pass response




(a)




(b)

Fig. 8. Post-layout simulated maximum-gain AFE frequency responses at −40 °C, 25 °C, and 125 °C at typical process for the programmable low-pass cutoff-frequency modes of (a) 120 kHz and (b) 180 kHz.

composed of a first-order HPF followed by a third-order low-pass filter (LPF). In conjunction with the external HPF before the PGA described in Section III-B, the cascaded response forms a second-order HPF. At the same time, the intrinsic LPF pole of the PGA contributes one additional order to the third-order LPF, resulting in an overall fourth-order low-pass response.

To achieve a high overall AFE gain without relying on a single high-gain stage, a fixed-gain (18 dB) filter stage is employed, thereby reducing the number of high-gain amplifiers, overall power consumption, and chip area. Fig. 7 shows a simplified schematic of the filter stage, which consists of a first-order active HPF, a second-order multiple-feedback LPF (MFB LPF), and a first-order passive LPF. The first-order HPF suppresses DC offset and low-frequency noise generated by the high-gain PGA. The HPF, implemented with an operational amplifier and passive components ($C_{S1}$, $R_{F1}$, and $C_{F1}$), has a cut-off frequency set to 4 kHz, matching that of the external HPF.

Furthermore, it offers an extensive cut-off frequency of 180 kHz, aligned with the PGA bandwidth option, enabling operation with transducers of different resonant frequencies. Table I provides the component values used, based on the preferred cutoff frequencies for the first-order HPF and third-order LPF.

To evaluate the AFE robustness over the automotive temperature range of -40°C to 125°C, post-layout frequency-

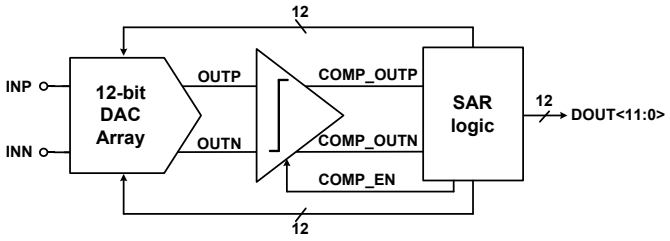
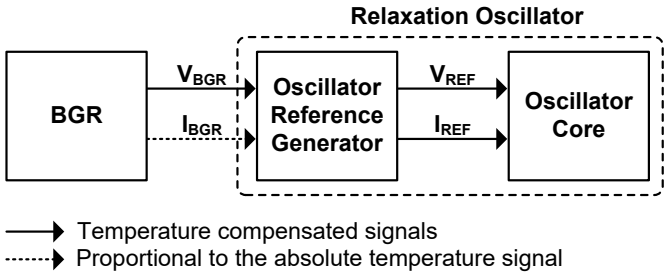
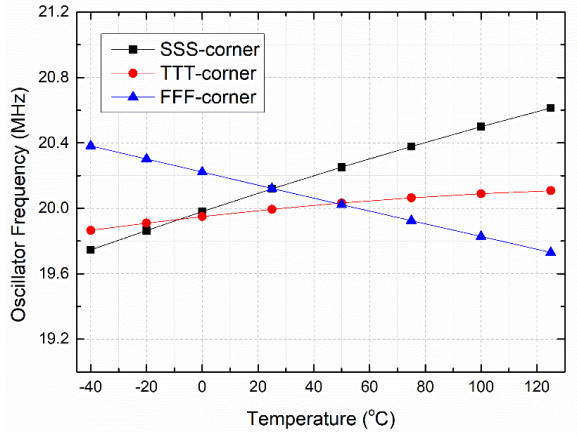



Fig. 9. Block diagram of the 12-bit SAR ADC.




(a)




(b)

Fig. 10. (a) The block diagram of the relaxation oscillator with temperature compensation and (b) simulated oscillation frequency variation versus temperature across process corners.

response simulations were performed. The AFE is designed to reduce temperature sensitivity through its passive-coupled HPF, which maintains a nominal cutoff near 4 kHz, and the PGA's ratio-matched on-chip resistors, which suppress first-order temperature drifts. As shown in Fig. 8, the simulated maximum-gain AFE responses for the 120-kHz and 180-kHz programmable low-pass cutoff modes keep the 58-kHz signal within the flat-gain region across the evaluated temperature range. These results confirm that the required in-band gain and bandwidth margins are preserved under automotive temperature variations.

### D. SAR ADC

To digitize the conditioned echo signals, a fully differential 12-bit SAR ADC is integrated at the end of the analog front-end. Fig. 9 illustrates the simplified block diagram of the ADC, which consists of a 12-bit digital-to-analog converter (DAC) array, a dynamic comparator, and SAR control logic. The SAR topology is selected for this ultrasonic sensor application because it provides high power efficiency and a minimal silicon footprint at the target sampling rate of 1.25 MS/s.

This sampling rate is chosen to oversample the 58-kHz narrowband echo signal, which relaxes the roll-off requirements of the preceding analog low-pass filters. Additionally, the 1.25-MS/s rate provides a high temporal resolution of 0.8 μs. This temporal precision is essential for accurate ToF estimation in the digital back-end, effectively supporting the system's overall ranging accuracy. Furthermore, the 12-bit resolution ensures that the quantization noise floor remains strictly below the amplified thermal noise level of the AFE. This prevents any degradation of the overall signal-to-noise ratio (SNR) prior to the digital processing.

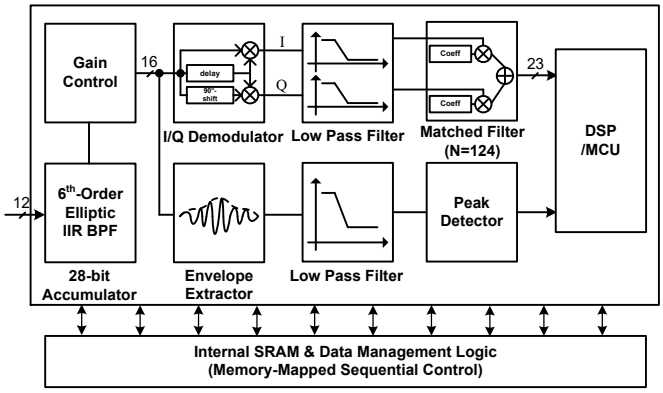



Fig. 11. Functional block diagram of the digital back-end.

### E. Relaxation Oscillator

To provide a stable global clock for the ADC and digital domain, a temperature-compensated relaxation oscillator is integrated [11]. Fig. 10(a) shows the conceptual block diagram. The reference generator combines complementary-to-absolute-temperature (CTAT) and proportional-to-absolute-temperature (PTAT) characteristics to produce temperature-independent reference signals ($V_{REF}$ and $I_{REF}$) for the oscillator core.

Because internal clock nodes are not connected to external test pads to avoid parasitic loading, the compensation circuit is verified via post-layout simulations. Fig. 10(b) presents the simulated oscillation frequency across process corners from -40°C to 125°C. The $I_{REF}/V_{REF}$ ratio remains constant, limiting the oscillator's frequency variation to under 4.3%. This frequency stability prevents asynchronous UART communication errors across the automotive temperature range.

## IV. Digital Back-end

As illustrated in the overall system architecture of Fig. 1, the DBE comprises several processing stages that operate on the ADC output to perform band-pass filtering, envelope extraction, peak detection, and π/4-DQPSK-based module identification. To execute the complex signal conditioning efficiently within a constrained area, the DBE employs a memory-mapped architecture utilizing the internal SRAM, as detailed in Fig. 11. This structure streams 12-bit ADC data into ring buffers, sequentially processing the 6th-order elliptic IIR filter and π/4-DQPSK demodulation stages.

A sixth-order elliptic infinite-impulse-response (IIR) filter serves as the front stage. To mitigate finite word-length effects, the internal data paths are strictly sized based on fixed-point bit-growth analysis. Specifically, the 12-bit ADC output is processed by the IIR filter using 28-bit internal recursive

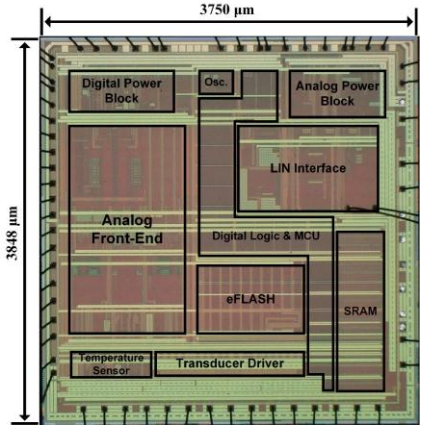



Fig. 12. Chip micrograph of the proposed distance detection ultrasonic sensor IC.

accumulators (14-bit integer, 14-bit fractional) to prevent overflow, yielding a 16-bit filtered output. This BPF signal exhibits a center frequency of 60 kHz, lower and upper cutoff frequencies of 55 kHz and 65 kHz, respectively, and a stopband attenuation exceeding 80 dB. Following the BPF, a digital-gain control block scales the signal to match the dynamic range of the subsequent processing stages.

The envelope extractor computes the windowed peak of the band-pass-filtered signal, with programmable window size and shift interval. It supports both absolute-value and half-wave rectification modes before peak selection. A first-order IIR LPF, implemented as an exponential moving average, suppresses residual high-frequency components to produce a smoothed envelope.

For module identification, a π/4-DQPSK I/Q demodulator extracts the phase differences from the BPF output. By encoding 2 bits per symbol, π/4-DQPSK halves the symbol rate to accommodate the narrow transducer passband. The demodulator employs a non-coherent delay-and-multiply architecture. A one-symbol digital delay line and a 90° phase-shift filter extract the differential I/Q components, eliminating the need for a carrier-recovery PLL and reducing hardware complexity.

Following demodulation, the matched filter performs cross-correlation to identify the transmitting module and extract ToF information. The reference coefficients utilize a length-31 Gold code, oversampled four times (N=124) to match the narrow transducer bandwidth. Gold codes are selected for their bounded cross-correlation properties, which suppress interference from non-matching modules and minimize false alarms, while providing a sharp auto-correlation peak for ToF estimation.

As illustrated in Fig. 11, the matched filter is implemented using a MAC architecture. Rather than employing 124 parallel multipliers, a single shared MAC unit sequentially multiplies the incoming 16-bit SRAM ring-buffer samples with the Gold code sequence stored in programmable on-chip registers. Accumulating over 124 cycles, this resource-shared approach minimizes the combinational logic area while sustaining the 1.25 MS/s throughput. To accommodate the correlation bit-growth, the MAC accumulator expands by $\log_2(124)=7$ bits above the 16-bit IIR output. By ensuring sufficient bit-widths

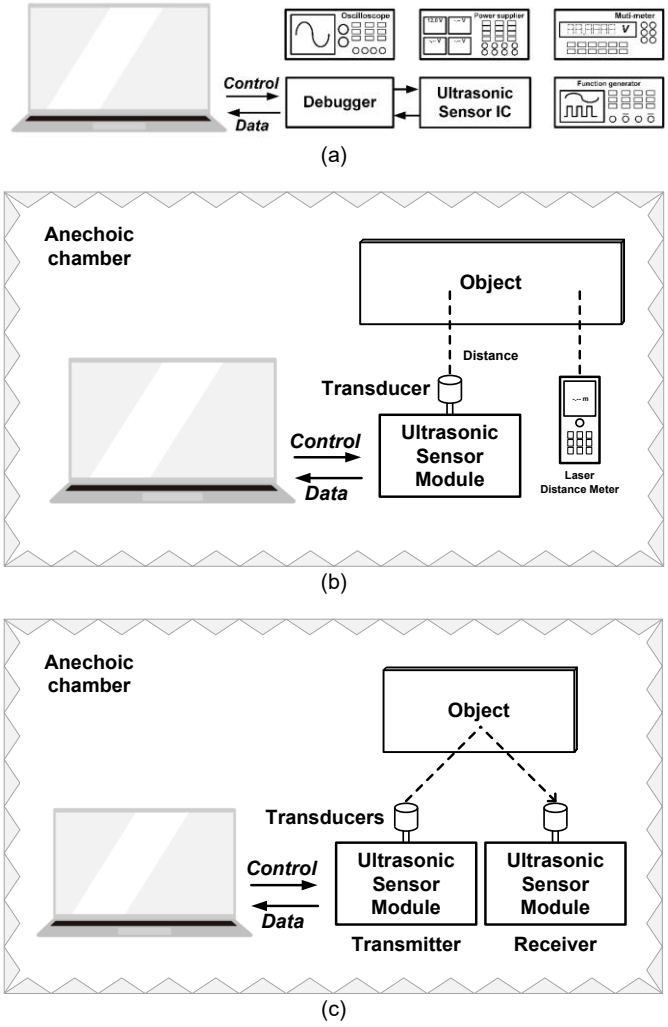



Fig. 13. Measurement setups for (a) ultrasonic sensor IC (b) ultrasonic sensor module, and (c) the indirect mode evaluation.

at these critical nodes, the hardware intrinsically avoids truncation errors, yielding a 23-bit correlation result that preserves the 20.9-dB theoretical processing gain.

The peak detector divides the envelope into 16 segments and, for each segment, determines the rising, maximum, and falling peak values. The detector is configurable; its thresholds, gain, and number of segments can be individually adjusted, enabling signal normalization and receiver noise suppression. An on-chip buffer stores the three largest local maxima extracted from the envelope.

When multiple ultrasonic sensor modules operate simultaneously, the goal is to detect only the signal from the intended module while rejecting interference from the others. Each module transmits a unique ID code embedded within its ultrasonic waveform. Owing to the narrow sensor bandwidth (approximately 2–3 kHz), PSK is more suitable than frequency-shift keying (FSK).

Specifically, transmitting a 124-symbol ID sequence at the required 7.25 kbps data rate with BPSK demands a 7.25 kHz main-lobe bandwidth, exceeds the transducer's approximately 3-kHz passband and causes inter-symbol interference (ISI). By encoding 2 bits per symbol, π/4-DQPSK halves the symbol rate to 3.625 kSymbols/s, reducing the single-sided main-lobe

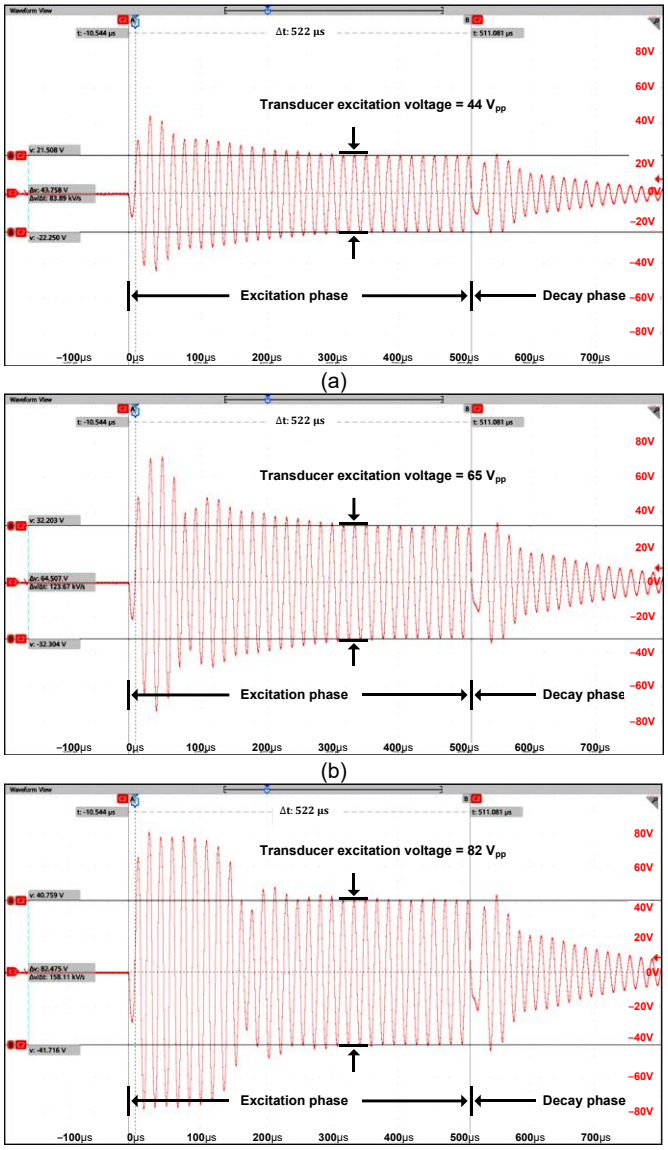



Fig. 14. Measured transducer excitation voltages when driving currents are (a) 155 mA, (b) 250 mA, and (c) 345 mA.

bandwidth to 3.625 kHz to accommodate the narrow passband.

Furthermore, unlike conventional BPSK or QPSK where phase transitions cross the origin (0V) and induce severe mechanical ring-down distortion, π/4-DQPSK avoids the origin via {±π/4, ±3π/4} transitions, maintaining a stable acoustic envelope. Although BPSK and QPSK typically require precise carrier synchronization, DQPSK is better suited to asynchronous operation and narrow bandwidth. Using π/4-DQPSK, the system performs I/Q demodulation to estimate differential phase. For this demodulator, a non-coherent delay-and-multiply architecture is adopted. A digital delay and a 90° phase-shift filter extract the phase differences without requiring a carrier-recovery PLL. The system then correlates the resulting symbol stream with the module's ID code to identify the transmitter and obtain distance information [12]–[14]. Furthermore, alternative parameter estimation frameworks for M-ary PSK signals, such as the finite-rate-of-innovation (FRI) approach, offer potential pathways for further enhancing symbol-level detection accuracy [15].

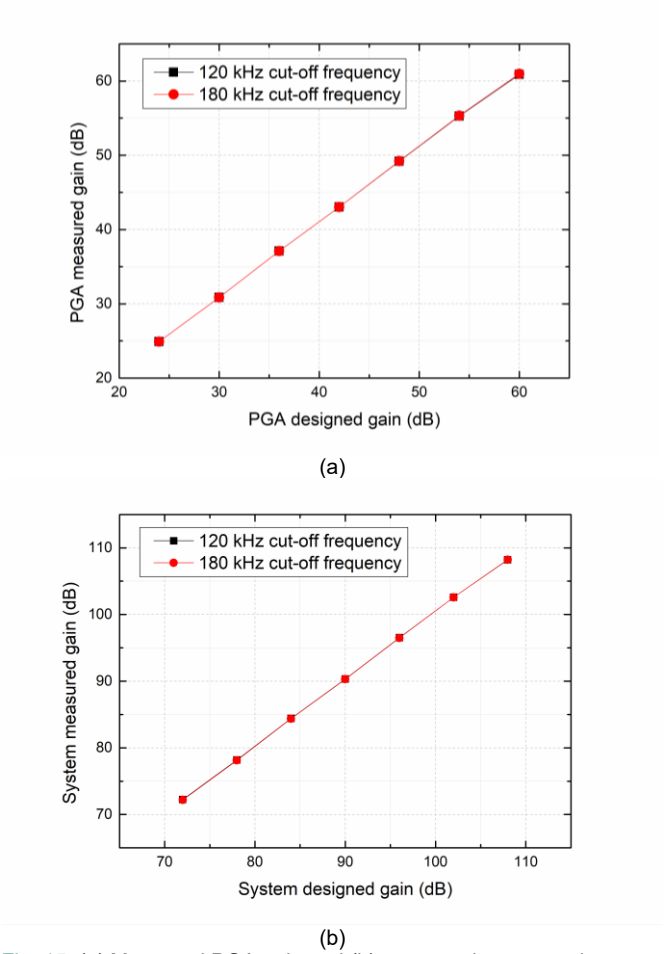



Fig. 15. (a) Measured PGA gain and (b) measured system gain.

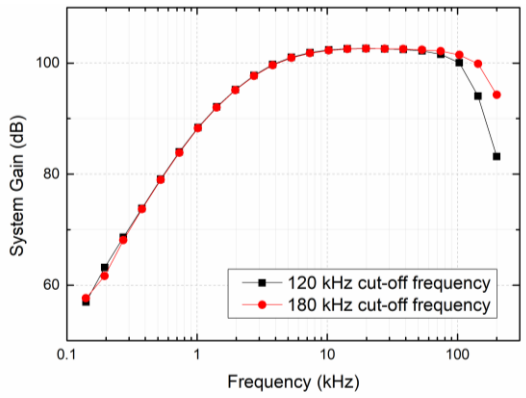



Fig. 16. Measured frequency response of the ultrasonic sensor IC.

## V. Experimental Results

### A. Measurement Setup

The chip micrograph of the proposed distance-detection ultrasonic sensor IC is shown in Fig. 12. The IC includes a LIN interface, power blocks, digital logic, an MCU, embedded flash (eFlash), static random-access memory (SRAM), and I/O pads; the total chip area is 14.43 mm². The overall system was evaluated using a custom-designed ultrasonic transducer. The key electrical and acoustic parameters of the transducer dictate the boundary conditions for the system evaluation. Specifically, the transducer features a nominal resonant frequency of 58 kHz

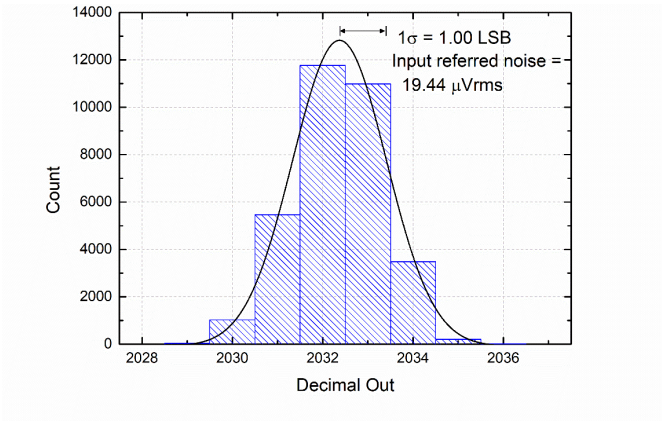



Fig. 17. Measured noise histogram of the ultrasonic sensor IC.

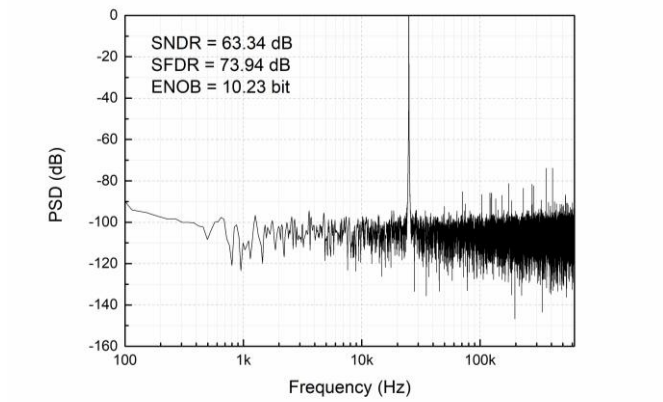



Fig. 18. Measured FFT result of ADC at 9.3 kHz input frequency.

and a static capacitance of 1.1 nF at 1 kHz, which are utilized to configure the LC resonance matching network. Furthermore, it has a maximum input voltage tolerance of 140 $V_{pp}$. To support the required detection range, the transducer provides a reflective sensitivity of 2.7 to 6.7 $mV_{pp}$ and exhibits a decay time ranging from 0.48 to 1.50 ms.

Fig. 13(a) illustrates the experimental setup used to characterize the proposed ultrasonic sensor IC. The setup includes a power supply for the IC and transformer, a function generator to produce sine-wave excitation signals, an oscilloscope, and a multimeter to measure outputs at multiple nodes. The on-chip MCU is connected to a personal computer to monitor and record the ADC and digital circuit outputs. Fig. 13(b) shows the measurement setup used to validate the object detection functionality of the ultrasonic sensor module. The target object was positioned along the transducer's acoustic axis. All measurements were performed in an anechoic chamber to minimize acoustic reflections from the surrounding walls, floor, and ceiling. The same setup was also used to measure the ringing frequency during the transducer's decay phase. The ID detection operation, which determines the object distance by integrating an ID code in the transmitted ultrasonic waveform, was verified using this setup. A laser distance meter was used as a reference instrument to measure the actual object distance.

### *B. Measurement Results of Ultrasonic Sensor IC*

Fig. 14 shows the measured secondary winding voltages of the transformer under different magnitudes of driving current from the transducer driver. In all cases, 58-kHz voltage signals,

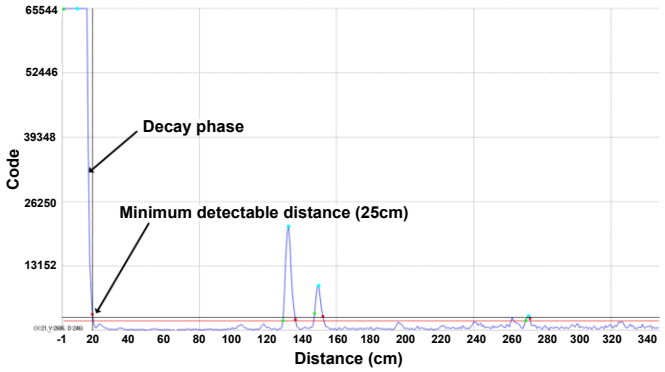



Fig. 19. Decay phase of transducer and minimum detectable distance of ultrasonic sensor module.

corresponding to the transducer's resonant frequency, are generated to excite the transducer. Peak-to-peak transducer voltages of 44 $V_{pp}$, 65 $V_{pp}$, and 82 $V_{pp}$ are observed for driving currents of 155 mA, 250 mA, and 345 mA, respectively. These results agree with (6), confirming that the excitation voltage is proportional to the transducer's driving current. Additionally, Fig. 14(a)–(c) depict the decay phase resulting from the residual energy stored in the transducer.

The input differential ultrasonic signal is significantly amplified by the PGA of the AFE, as shown in Fig. 15(a). PGA gain is adjustable between 24 dB and 60 dB in 6 dB increments. The gain values are linear for all gain settings, with an error rate of less than 1.1 %. Fig. 15(b) presents the measurement results for the system total gain, including both the AFE and the digital gain. Including the filter gain of 18 dB and digital gain of 30 dB, the system gain can reach a maximum of 108 dB.

Fig. 16 shows the measured frequency response when the total system gain is set to 102 dB. The response was obtained by sweeping the input frequency of a sine-wave signal applied to the AFE using a function generator. The passband response varies depending on the selected cutoff-frequency option. The measured gain within the transducer's resonant frequency band is 102 dB, consistent with the designed system gain. Based on the PGA gain and 30-dB digital gain, the fixed filter-stage gain is determined to be 18 dB. The HPF cut-off frequency is 3.6 kHz, and the LPF cut-off frequency is 182.9 kHz. For the BPF response, the HPF exhibits a second-order slope of +40 dB/dec, while the LPF shows a fourth-order slope of -80 dB/dec. As the AFE is optimized for ultrasonic operation within the 30–180 kHz range, which already encompasses the entire signal band of interest, and the cascaded filter structure inherently provides sufficient out-of-band attenuation, additional high-frequency measurements beyond 182.9 kHz were unnecessary because they do not affect the in-band response or system performance.

Fig. 17 shows the measured overall noise level of the proposed ultrasonic sensor IC. The noise generated by the AFE is measured with both transducer terminals grounded. When the AFE gain is set to 42 dB, the measured output standard deviation of approximately 1.00 least significant bit (LSB) corresponds to an input-referred noise level of 19.44 $\mu V_{rms}$. This low measured input-referred noise, together with the temperature-stable gain and bandwidth characteristics verified in Fig. 8, supports the required SNR margin for subsequent ToF estimation and module-ID detection.

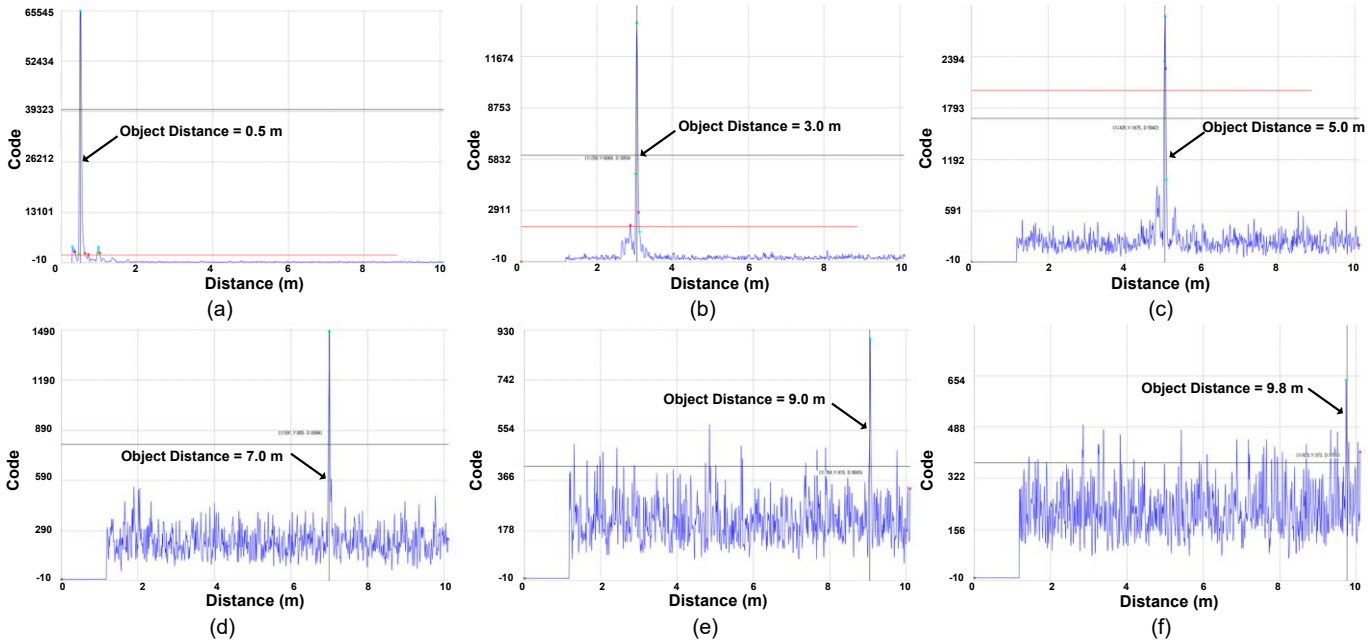



Fig. 20. Detection of an object placed at (a) 0.5 m, (b) 3.0 m, (c) 5.0 m, (d) 7.0 m, (e) 9.0 m, and (f) 9.8 m.

Fig. 18 shows the measured fast Fourier transform (FFT) spectrum of the ADC. A differential sinusoidal input signal with an amplitude of 9 $V_{pp}$ and a frequency of 9.3 kHz is applied using a function generator. The ADC operates at a sampling rate of 1.25 MS/s during the measurement. According to the FFT analysis, the signal-to-noise and distortion ratio (SNDR) is 63.34 dB, while the spurious-free dynamic range (SFDR) is 73.94 dB. These results correspond to an effective number of bits (ENOB) of 10.23 bits.

### C. *Measurement Results of Ultrasonic Sensor Module*

The distance detection performance of the ultrasonic sensor module is evaluated using the experimental setup shown in Fig. 13(b). During the distance measurement, the transducer is driven at its resonance frequency of 58 kHz with a current of 273.7 mA. The AFE gain is set to 72 dB, and the digital gain to 18 dB, resulting in a total system gain of 90 dB. With the ADC sampling the ultrasonic signal at eight times the 58-kHz resonance frequency, the module achieves a distance resolution of 0.73 mm. As shown in Fig. 19, the transducer's decay phase introduces a blind zone in which the reflected ultrasonic signal cannot be detected. Consequently, the minimum detectable distance of the ultrasonic sensor module is approximately 25 cm, corresponding to the end of the transducer's ringing. To evaluate the maximum detectable distance, the distance to the target is gradually increased. During this test, the digital gain for the decay phase was set to zero to facilitate accurate identification of the received echo signal. Fig. 20 shows that the reflected ultrasonic signal is clearly detected for object distances ranging from 50 cm to 9.8 m. At the maximum tested distance of 9.8 m, the received signal remains distinguishable from the noise floor.

The ID detection process is designed to identify only the signal transmitted by the corresponding module while rejecting signals from other modules when multiple ultrasonic sensor modules operate simultaneously. Each module embeds a unique ID code within its transmitted ultrasonic signal. Utilizing the π/4-DQPSK scheme, I/Q demodulation is performed to decode the phase difference of the signal. The distance information is then extracted by correlating the received signal with the transmitted ID code. To optimize hardware resources, the matched filter employs a resource-shared architecture that leverages the internal SRAM for sequential correlation, as shown in Fig. 11. In Fig. 21(a), the received and transmitted ID codes match, resulting in a distinct correlation peak at 2 m, confirming correct distance detection. In contrast, Fig. 21(b) shows no correlation peak because the received signal does not contain the ID code transmitted by the module itself.

These matched- and mismatched-ID measurements validate the system-level function that distinguishes the proposed architecture from conventional ToF-only ICs. While the envelope-detection path robustly determines the echo arrival time regardless of the transmitter, the concurrent DQPSK correlation path authenticates whether the detected acoustic waveform carries the assigned module ID. The absence of a correlation peak for the mismatched code (Fig. 21(b)) confirms that the internal digital back-end successfully rejects unassigned waveforms. Obtaining these code-selective correlation results alongside the 9.8-m maximum detectable distance demonstrates that the highly constrained hardware co-design integrates module discrimination while maintaining the long-range echo sensitivity of the shared mixed-signal acquisition path.

In addition to the standard direct mode, the proposed IC supports an indirect mode to overcome the short-range blind zone caused by the transducer's mechanical ring-down. This mode employs two separate sensor boards spaced 10 cm apart to establish a separate signal path, as shown in Fig. 13(c). Within the receiver IC, the internal transmit driver is electrically disabled. Because the receiving transducer is isolated from the high-voltage excitation, it experiences no mechanical ring-down, allowing the AFE's programmable gain amplifier to maintain linearity from the start of the

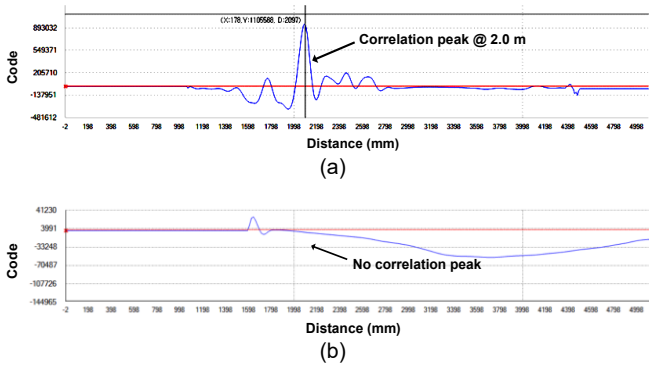



Fig. 21. Correlation results of ID detection at a distance of 2 m for (a) matched ID code and (b) mismatched ID code.

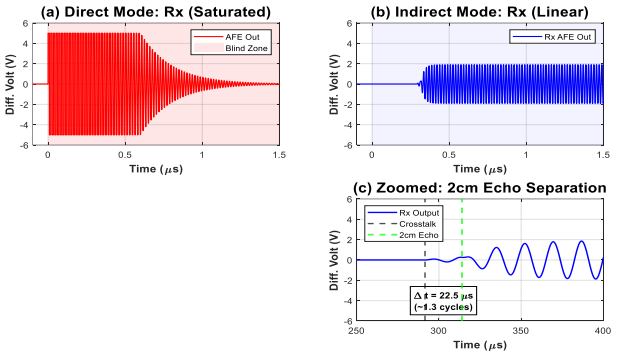



Fig. 22. Analysis of receiver saturation and 2-cm echo separation mechanism: (a) AFE saturation in direct mode, (b) linear operation in indirect mode, and (c) 22.5 μs echo separation margin

measurement.

Based on this saturation-free operation, the system is theoretically capable of resolving short-range targets down to a 2 cm object distance, as established by the geometric path analysis described below. The detailed mechanism and timing diagram for this close-range detection are illustrated in Fig. 22. In this 10-cm-spaced indirect mode setup, the transmitting and receiving transducers are aligned along the same axis. For a target positioned 2 cm in front of the midpoint of the sensor pair, the acoustic echo path from the transmitter to the target and back to the receiver is calculated as $2 \times \sqrt{(5\ \text{cm})^2 + (2\ \text{cm})^2} \approx 10.77$ cm. At a speed of sound of 343 m/s, this corresponds to a time-of-flight of approximately 314 μs. This arrival time provides a sufficient temporal margin of approximately 22.5 μs to be resolved from the direct board-to-board crosstalk. The experimental results in Fig. 23 validate the practical operation of the indirect mode by showing a clear correlation peak for an object located at 10 cm, which is within the 25-cm blind zone of the direct mode. Because direct measurement at 2 cm was limited by the physical constraints of the laboratory setup, the experimentally verified minimum detectable distance in this work is 10 cm. The 2-cm value is therefore reported as a theoretical limit derived from the geometric path analysis and the 22.5-μs echo separation margin. This mode is commonly used in automotive parking-assist systems to enable close-range detection and to avoid self-interference among multiple sensors.

Table II compares the proposed ultrasonic sensor module

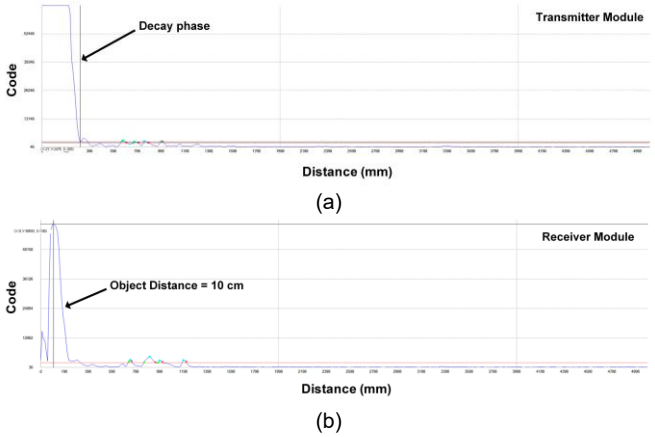



Fig. 23. Detection of an object in indirect mode is shown by (a) the transmitter module and (b) the receiver module.

with commercial alternatives. The proposed ultrasonic sensor IC was implemented in a 130-nm CMOS technology and is designed to operate directly from a 12-V automotive battery. The sensing module achieves a maximum detection range of 9.8 m. In the indirect mode, the experimentally verified minimum distance is 10 cm, while the 2-cm value represents the theoretical limit derived from the geometric path analysis and echo-separation margin. At a target distance of 1 m, the measured ranging error is 2.51 $\text{mm}_{\text{rms}}$. Furthermore, the system incorporates an ID detection scheme that allows discrimination of ultrasonic signals originating from different modules. This comparison highlights that the proposed IC uniquely combines long-range ToF sensing with module-ID detection using a shared mixed-signal acquisition path. The fabricated IC occupies an area of 14.43 $\text{mm}^2$ and dissipates 399.7 mW, excluding the transducer driver's current consumption. Internally, the analog front-end (AFE) and digital domain consume 90.95 mW at 3.3 V and 8.63 mW at 1.5 V, respectively, with the remainder dissipated by internal LDOs.

In automotive applications, long-range detection and signal integrity are prioritized over strict power reduction. Thus, LDOs are employed to provide the highly stable, noise-free supply required for the 9.8-m range, inherently dominating the total power. The use of LDOs is a deliberate architectural choice to comply with strict automotive EMI constraints and minimize the module size by eliminating bulky external inductors required for switching converters. This analog overhead is balanced by the memory-mapped SRAM architecture, which strictly limits the digital power to 8.63 mW. To evaluate energy efficiency, a system-level Walden figure of merit ($\text{FoM}_\text{W}$) is calculated as $P_{\text{total}}/(2\times\text{BW}\times 2^{\text{ENOB}})$, where $P_{\text{total}}$=399.7mW denotes the total IC power excluding the driver, BW=3 kHz is the 3-dB signal bandwidth centered at 58 kHz, and the effective number of bits (ENOB) is derived from the measured input-referred noise of 19.44 $\mu\text{V}_{\text{rms}}$ relative to the full-scale AFE input range. The proposed design achieves an $\text{FoM}_\text{W}$ of 14.12 nJ/conv-step. This comparison highlights the superior performance of the proposed ultrasonic sensor module compared to commercially available options.

## VI. Conclusion

This paper presents a novel ultrasonic sensor IC for

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER ULTRASONIC PARKING ASSIST DISTANCE DETECTORS

| | This work | On Semiconductor NCV75215 2017 [16] | Elmos E524.14 2015 [17] | Texas Instruments PGA460 2017 [18] | | L. Wu et al. [19] |
|---|---|---|---|---|---|---|
| Process | 130 nm | N/A | N/A | N/A | | 180 nm |
| Sensing Method | Time-of-Flight | Time-of-Flight | Time-of-Flight | Time-of-Flight | | Time-of-Flight |
| Typical Operating Voltage | 12 V | 12 V | 13.5 V | 14 V | | N/A |
| Internal Analog Voltage | 5 V | 3.3 V | 3.3 V | 1.8 V | | N/A |
| Range of Transducer Frequencies | 30 – 120 kHz<br>30 – 180 kHz | 35 – 90 kHz | 30 – 80 kHz | 30 – 80 kHz | 180 – 480 kHz | 40/192 kHz |
| Transducer Driver Adjustment Current | 155 – 404 mA | 50 – 350 mA | 188 – 518 mA | 50 – 500 mA | | N/A |
| Transducer Receiver Gain | 42 – 108 dB | 50 – 110 dB | 56.5 – 88 dB | 32 – 90 dB | | 19 – 73 dB |
| ADC Resolution | 12-bit | 8-bit | 8-bit | 12-bit | | 10-bit |
| Minimum Detection Distance | 25 cm<br>(normal mode)<br>2 cm**<br>(indirect mode) | 250 cm | 15 cm | 30 cm | 5 cm | 10 cm |
| Maximum Detection Distance | 9.8 m<br>@ Transducer Driver Current = 273.7 mA | 4.5 m | 5 m | 5 m | 1 m | 7 m |
| Distance Error | 2.51 $mm_{rms}$<br>@ 1 m | N/A | N/A | N/A | | 7.3 $mm_{rms}$<br>@ 0.4 m |
| ID Detection | O | X | X | X | | X |
| Indirect Mode | O | O | X | X | | X |
| Chip Area | 14.43 $mm^2$ | N/A | N/A | N/A | | 32.5 $mm^2$ |
| Power Consumption excluding Transducer Driver | 399.7 mW | 96 mW | 135 mW | 168 mW | | 142.3 mW |
| Walden FoM* | 14.12 nJ/Conv. | 16.5 nJ/Conv. | 9.23 nJ/Conv. | 25.41 nJ/Conv. | | N/A |

*$FoM_W = P_{total}/(2 \times BW \times 2^{ENOB})$
**Theoretical limit; experimentally verified at 10 cm.

automotive parking-assist systems. The IC uses ToF measurements of ultrasonic waves to determine the distance to surrounding objects. It integrates an ultrasonic transducer driver, an AFE for signal conditioning, an ADC, and a DBE for distance computation and ID detection.

Since the reflected ultrasonic signal attenuates with distance, both high system gain and a high SNR are required for reliable operation. To accommodate ultrasonic-band signals, a wide-bandwidth AFE was designed. The high-gain, wide-bandwidth PGA is implemented using a differentially compensated amplifier architecture. Unwanted out-of-band noise is filtered in the analog domain to enhance the overall SNR. Because the propagation velocity of ultrasound in air varies with temperature, an on-chip temperature sensor is integrated to enable temperature compensation and improve ranging accuracy [20].

Experimental results obtained from a prototype module demonstrate the excellent performance of the proposed IC. The prototype demonstrates a maximum detectable distance of 9.8 m. In indirect mode, object detection was experimentally verified at 10 cm, which lies within the blind zone of the direct mode, while the 2-cm minimum distance represents a theoretical limit derived from geometric path analysis. A ranging error of 2.51 $mm_{rms}$ was measured at an object distance of 1 m. In addition, the ID-detection function enables reliable discrimination of ultrasonic signals from multiple modules operating simultaneously.

Fabricated in a 130-nm CMOS process, the proposed IC operates directly from a 12-V automotive battery, occupies 14.43 $mm^2$, and dissipates 399.7 mW, excluding the transducer driver current. The measured FoM is 14.12 nJ/conv-step, confirming the high energy efficiency of the proposed architecture. These results verify the effectiveness of the proposed design and demonstrate its potential to advance next-generation automotive parking-assistance systems.

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